# U S E R ' S  M A N U A L

C&H Technologies, Inc. <> 445 Round Rock West Drive <> Round Rock, TX 78681 <> www.chtech.com

# HIGH SPEED APERTURE A/D M-MODULE

## MODEL M228

Document Part No: 11030504

## COPYRIGHT



A Reader's Comment Form is provided at the back of this publication. If this form has been removed address comments to:

C&H Technologies, Inc.
Technical Publications
445 Round Rock West Drive
Austin, Texas 78681-5012

Or visit our web site for support information at:

http://www.chtech.com.

## AMENDMENT NOTICE

C&H Technologies, Inc. makes every attempt to provide up-to-date manuals with the associated equipment. Occasionally, changes are made to the equipment wherein it is necessary to provide amendments to the manual. If any amendments are provided for this manual they are printed on colored paper and will be provided with the module and manual. Manual updates may also be found on out web site at www.chtech.com.

## NOTE

The contents of any amendment may affect operation, maintenance, or calibration of the equipment.

# INTRODUCTION

This manual describes the operation and use of the C&H Model M228 High Speed Aperture A/D (Part Number 11030500). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, LXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

TABLE OF CONTENTS


1.0 GENERAL DESCRIPTION ..... 1
1.1 PURPOSE OF EQUIPMENT ..... 1
1.2 SPECIFICATIONS OF EQUIPMENT ..... 1
1.2.1 Key Features ..... 1
1.2.2 Specifications ..... 2
1.2.3 Mechanical ..... 6
1.2.4 Bus Compliance ..... 6
1.2.5 Applicable Documents ..... 6
1.2.6 Credits ..... 6
2.0 INSTALLATION ..... 7
2.1 UNPACKING AND INSPECTION ..... 7
2.2 HANDLING PRECAUTIONS ..... 7
2.3 INSTALLATION OF M MODULES ..... 7
2.4 PREPARATION FOR RESHIPMENT ..... 8
3.0 FUNCTIONAL DESCRIPTION ..... 9
3.1 OVERVIEW ..... 9
3.1.1 Programmable Divider ..... 9
3.1.2 Self test and Calibration Logic ..... 9
3.1.3 References ..... 9
3.1.4 Instrumentation Amplifier (IA) ..... 9
3.1.5 Anti-Aliasing Filter ..... 10
3.1.6 Programmable Gain Amplifier (PGA) ..... 10
3.1.7 Analog Digital Converter (ADC) ..... 10
3.1.8 Aperture Comparator ..... 10
3.1.9 FIFO ..... 10
3.1.10 32-Bit Timestamp ..... 11
3.1.11 Clock/Run Control ..... 11
3.1.12 On-board Oscillator ..... 11
3.1.13 External Inputs and Control ..... 11
3.1.14 External Outputs and Control ..... 11
3.1.15 M-Triggers & Control ..... 11
3.1.16 Calibration ..... 12
3.2 INPUT/OUTPUT SIGNALS ..... 12
3.3 CONFIGURATION AND IDENTIFICATION ..... 13
3.3.1 Programming Registers ..... 13
3.3.2 M-Module Identification PROM ..... 28
4.0 OPERATION ..... 29
4.1 A/D CONVERSION ..... 29
4.2 VALUE-TIME PAIR STORAGE ..... 29
4.3 APERTURE WINDOWS ..... 30
4.3.1 Aperture Mode 0 ..... 30
4.3.2 Aperture Mode 1 ..... 30
4.3.3 Aperture Mode 2 ..... 31
4.3.4 Aperture Mode 3 ..... 31

4.3.5 Aperture Mode 4 ..... 31
4.3.6 Aperture Mode 5 ..... 31
4.3.7 Aperture Mode 6 ..... 31
4.4 FILTER SELECTION ..... 32
4.5 CALIBRATION ..... 33
4.6 ID PROM ..... 34

LIST OF APPENDICES

APPENDIX A: CONNECTORS ..... A-1

LIST OF FIGURES

Figure 1. Frequency Response - Elliptic Filter ..... 4
Figure 2. Frequency Response - Bessel Filter ..... 4
Figure 3. Frequency Response - Bypass ..... 4
Figure 4. Transient Response - Elliptic Filter ..... 5
Figure 5. Transient Response - Bessel Filter ..... 5
Figure 6. Transient Response - Bypass ..... 5
Figure 7. M-Module Installation ..... 7
Figure 8. Functional Block Diagram ..... 9
Figure 9. Programming Registers ..... 14
Figure 10. ID PROM Access Routine ..... 34

Figure A-1. M/MA Interface Connector Configuration ..... A-1
Figure A-2. Front Panel Coax D-SUB Connector Configuration ..... A-2

LIST OF TABLES

Table I. Register Address Map ..... 13
Table II. M-Module EEPROM IDENT Words ..... 28
Table III. EEPROM Calibration Data Format ..... 33
Table IV. Single Calibration Entry Format ..... 33

## 1.0 GENERAL DESCRIPTION

The M228 is a 1MSPS 14-bit A/D converter module that samples and selectively stores differential analog signals along with a 32-bit time stamp at a rate up to 1MSPS. The module has the ability to convert and store all data at the specified sample rate or selectively store input values that exceed the range of the programmed aperture window. This technique provides extensive real-time data compression and data extraction for transient type input signals

The module conforms to the ANSI/VITA 12-1996 standard for M-modules, which allows it to be used in a variety of platforms, including VXI, LXI, PXI, VME, PCI, cPCI, and Ethernet, with the use of an M-module carrier.

### 1.1 PURPOSE OF EQUIPMENT

This instrument is designed for data acquisition applications required in industrial test and measurement systems. The instrument allows high speed (1MSPS) data acquisition and analysis of transient analog signals without massive amounts of data being stored.

### 1.2 SPECIFICATIONS OF EQUIPMENT

#### 1.2.1 Key Features

- 14-Bit Resolution
- Up to 1MSPS
- Bipolar Differential Input
- 32-Bit Timestamp
- 32Meg Deep Sample FIFO in Value-Time Pair storage mode
- 64Meg Deep Sample FIFO in Value Only storage mode
- Flexible Real-time Data Storage Modes with external real-time change capability
- Capture Till Full and Continuous Capture Mode
- Continue Time-Stamping while Capture Disabled
- External “Data Stored” signal
- Two Programmable Anti-aliasing Filters (one Bessel response and the other a linear phase elliptic response) plus a bypass mode
- Programmable Gain (front-end 1, 2, 5, or 10 and back-end 1, 2. 5, 10, 20, 50, or 100)
- Programmable 10:1 Voltage Divider
- ±60V Input Range
- 10MΩ Input Impedance

## 1.2.2 Specifications

**MAXIMUM RATINGS**

| Parameter | Condition | Rating | Units |
|---|---|---|---|
| Operating Temperature | | 0 to +50 | °C |
| Non-Operating Temperature | | -40 to +71 | °C |
| Humidity | non-condensing | 5 to 95 | % |
| Power Consumption | +5V<br>+12V<br>-12V | 485 (typ), 500 (max)<br>40 (typ), 100 (max)<br>80 (typ), 150 (max) | mA<br>mA<br>mA |
| Auxiliary Power Supply Current | +5V<br>+12V<br>-12V | 500<br>100<br>100 | mA<br>mA<br>mA |
| Voltage on Analog Inputs (AIN0+/-) | input connector limitation | ± 60 | V |
| Voltage on External Inputs (FPINA/B) | no damage, power off<br>no damage, power on | ± 40<br>± 36 | V<br>V |

**SPECIFICATIONS** (full operating temperature, unless otherwise specified)

| Parameter | Conditions | Limits | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **A/D Converter** | | | | | |
| Resolution | no missing codes | | | 14 | bits |
| Integral Linearity Error | | -1 | ±0.3 | +1 | LSB |
| Differential Linearity Error | | -1 | | +1 | LSB |
| Zero Error | before calibration | -15 | | +15 | LSB |
| Full Scale Error | before calibration | -20 | | +20 | LSB |
| Zero Error Drift | | | | 0.1 | mV/°C |
| Full Scale Error Drift | | | | 0.1 | mV/°C |
| Throughput | Warp Mode [1]<br>Normal Mode | 0.001<br>0 | | 1<br>800 | MSPS<br>KSPS |
| Signal to Noise Ratio | | | 85.5 | | dB |
| **Signal Input Conditioning** | | | | | |
| Input Range | normal (G = 1)<br>÷10 active (G = 1) | -10<br>-60 | | +10<br>+60 | V<br>V |
| Common Mode Voltage Range | | ±13 | | | V |
| Common Mode Rejection Ratio | dc to 50KHz | 80 | | | dB |
| Input Impedance | differential<br>common-mode<br>÷10 active | 20<br>10<br>10 | | | MΩ<br>MΩ<br>MΩ |
| Divider | programmable (1 or ÷10) | 1 | | 0.1 | V/V |
| Gain | overall<br>front end (1, 2, 5, or 10)<br>back end (1, 2. 5, 10, 20, 50, or 100) | 1<br>1<br>1 | | 1000<br>10<br>100 | V/V<br>V/V<br>V/V |
| Filter Cutoff Frequencies | Elliptic, programmable in binary steps<br>Bessel, programmable in binary steps | 1.6<br>0.3 | | 416<br>88 | KHz<br>KHz |
| Filter Response | See Frequency & Transient Response Curves (Figure 1 - Figure 6) | | | | |
| Group Delay | Elliptic, $f_C$ = 104KHz<br>Bessel, $f_C$ = 88KHz | 11.7<br>6 | 12<br>7 | 14.2<br>8 | µs<br>µs |

**SPECIFICATIONS** (continued)

| Parameter | Conditions | Limits | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Internal Sample Clock** | | | | | |
| Accuracy | | | | ±0.01 | % |
| Frequency | incremental (see note 3) | 10Hz | | 1 | MHz |
| Jitter | | | | ±500 | ps |
| **Calibration References** | | | | | |
| Accuracy | ±0.5V<br>±10V | -0.35<br>-0.1 | | 0.35<br>0.1 | %<br>% |
| Temperature Coefficient | ±0.5V<br>±10V | | | 25<br>50 | ppm/°C<br>ppm/°C |
| **External Inputs (FPINA & FPINB)** | | | | | |
| Input Threshold | programmable | 0 | | +5.0 | V |
| Input Impedance | programmable for 50Ω or<br>Hi-Z | 45<br>19K | 50 | 55 | Ω<br>Ω |
| Pulse Width | | 5 | | | ns |
| Frequency | see note 4 | | | 50 | MHz |
| **External Outputs (FPOUTA & FPOUTB)** | | | | | |
| Driver Type | Two 74ABT125 outputs in parallel with a 25Ω series resistor | | | | |
| Output High Voltage | $V_{OH}$ at -6ma<br>$V_{OH}$ at -64ma | 2.5<br>2.0 | | | V<br>V |
| Output Low Voltage | $V_{OL}$ at 128ma | | | 0.55 | V |

Specification Notes:

1. In Warp Mode, the time between conversions must not exceed 1ms.
2. Relative to gain at $0.1f_C$.
3. The internal clock rate is 1MHz. Sixteen programmable prescalers allow the internal sample rates to vary from 10Hz to 1MHz.
4. This is the maximum frequency that the input logic can accept. The maximum functional frequency is limited by the use of the input signal.

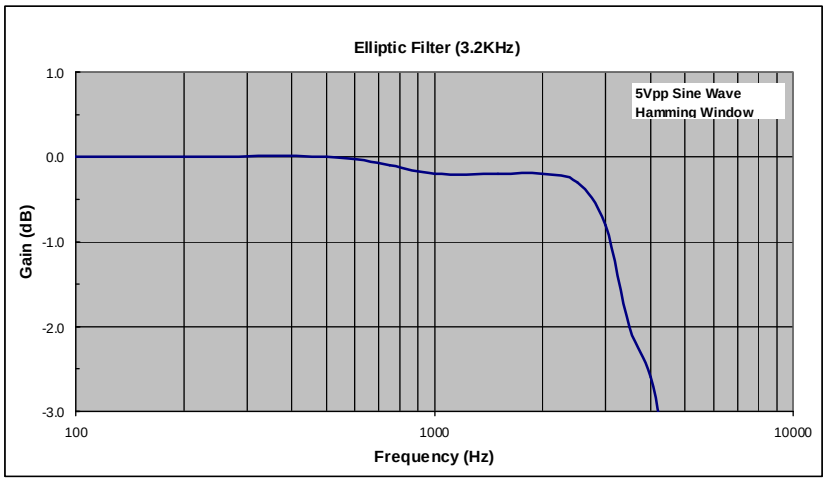



**Figure 1. Frequency Response - Elliptic Filter**

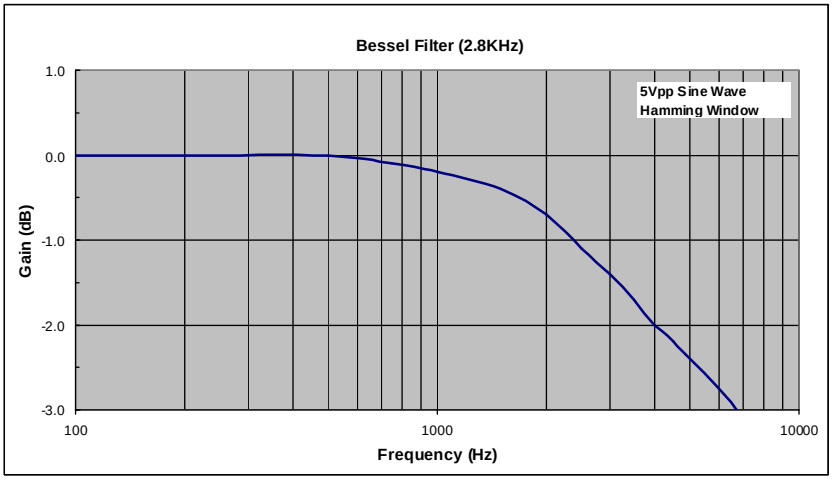



**Figure 2. Frequency Response - Bessel Filter**

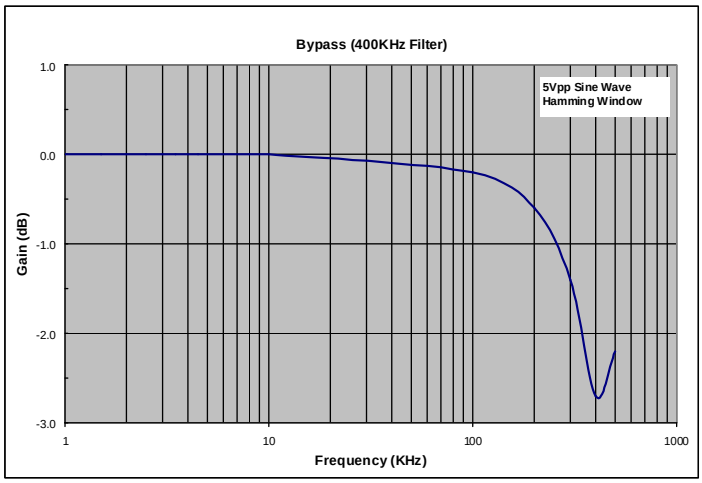



**Figure 3. Frequency Response - Bypass**

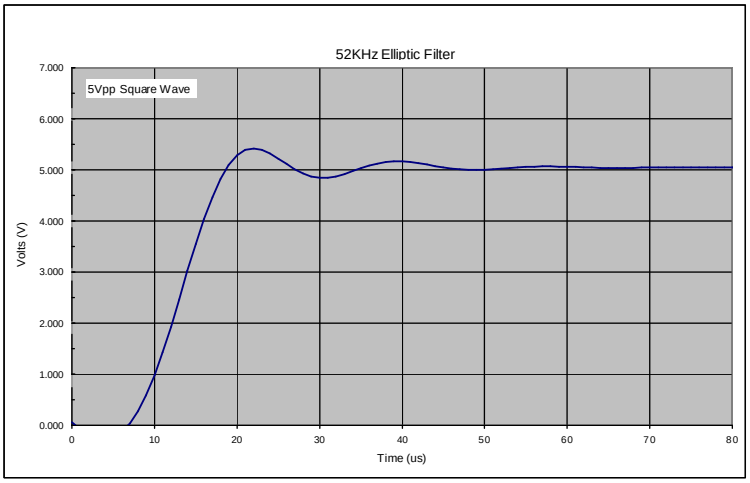



**Figure 4. Transient Response - Elliptic Filter**

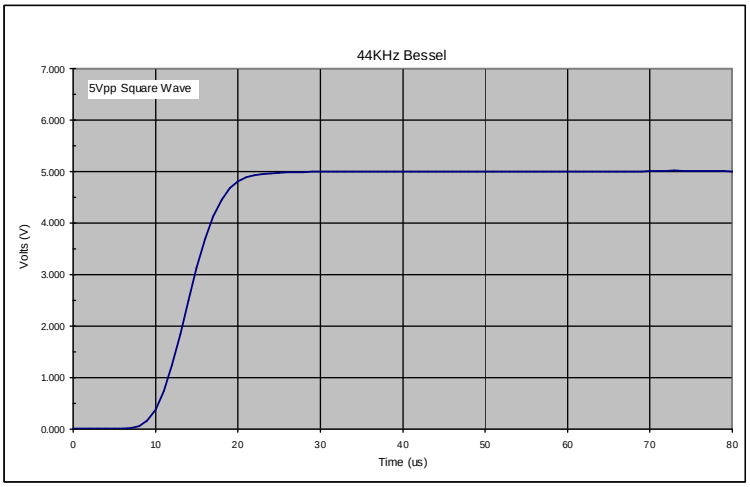



**Figure 5. Transient Response - Bessel Filter**

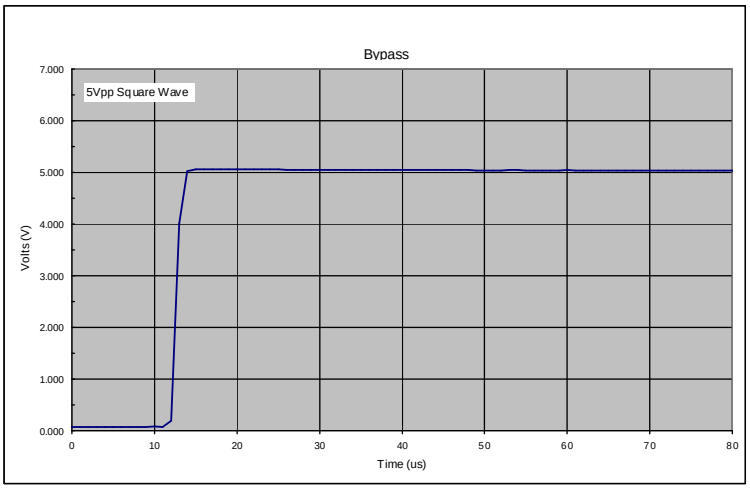



**Figure 6. Transient Response - Bypass**

### 1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (106.2 mm) wide.

### 1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules. The module also supports the optional IDENT and VXI-IDENT functions.

| | |
|---|---|
| Module Type: | M-Module |
| Addressing: | A08 |
| Data: | D16, D32 |
| Interrupts: | INTC (ROAK with vector) |
| Burst: | not supported |
| DMA: | not supported |
| Triggers: | MTRGA & MTRGB |
| Identification: | IDENT and VXI-IDENT |
| Manufacturer ID: | $0FC1_{16}$ |
| Model Number: | $00E4_{16}$ (228 dec.) |
| VXI Model Code: | $0FD4_{16}$ (M228) |

### 1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, www.vita.com

### 1.2.6 Credits

The following open source code was used in the design of this module:

1. I2CWB Wrapper (C) Victor Lopez Lorenzo under LGPL license
2. WISHBONE rev.B2 compliant synthesizable I2C Slave model (C) 2001 Richard Herveille richard@asics.ws under LGPL license

## 2.0 INSTALLATION

### 2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

### 2.2 HANDLING PRECAUTIONS

The M228 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

### 2.3 INSTALLATION OF M MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M-Module together with the connector on the carrier as shown in Figure 7. Secure the module through the holes in the bottom shield using the original screws.

**CAUTION: M-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M-Module and carrier.**

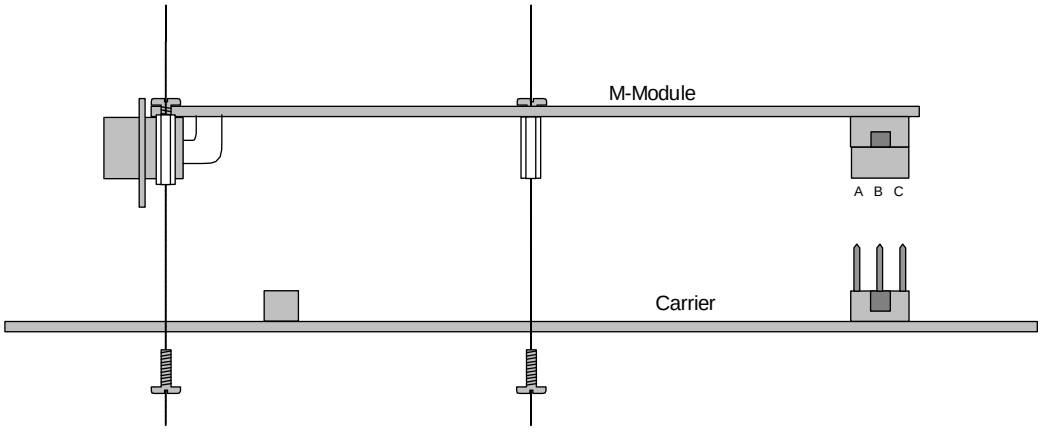



**Figure 7. M-Module Installation**

## 2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 OVERVIEW

A simplified functional block diagram of the module is shown in Figure 8.

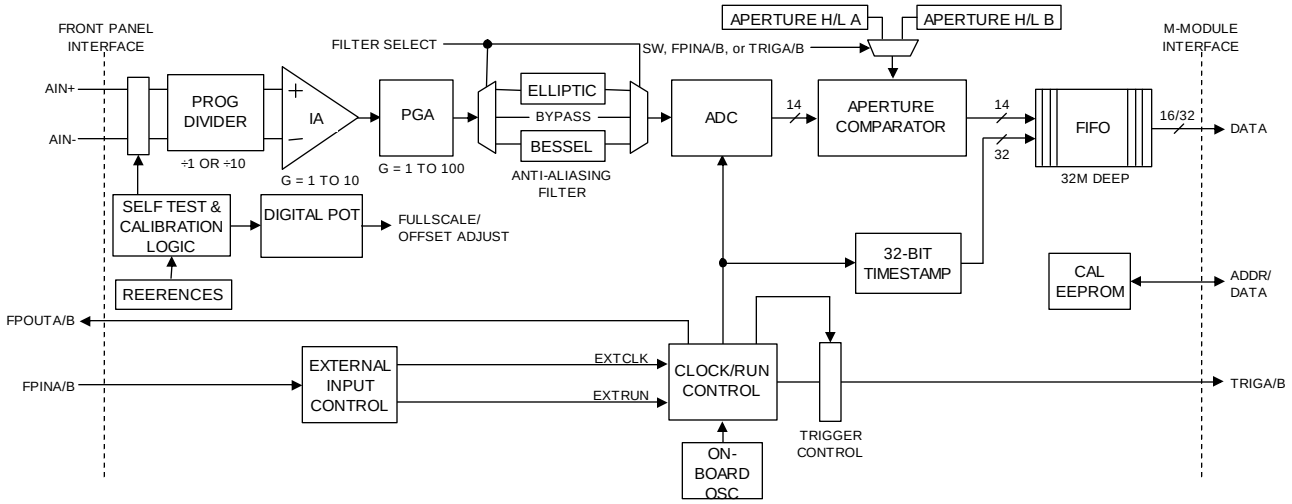



**Figure 8. Functional Block Diagram**

#### 3.1.1 Programmable Divider

The programmable divider allows the input voltage to be divided by ten in order to handle input voltage levels up to 60V.

#### 3.1.2 Self test and Calibration Logic

The self test and calibration logic can insert a reference signal at the inputs of the instrumentation amplifier. This reference signal can be used to self test or calibrate the unit.

#### 3.1.3 References

Several references are provided to allow internal reference calibration and self-test.

#### 3.1.4 Instrumentation Amplifier (IA)

The instrumentation amplifier provides differential input signal buffering and conditioning. This amplifier also provides a programmable (front end) gain of 1, 2, 5 or 10.

### 3.1.5 Anti-Aliasing Filter

Two types of anti-aliasing filters and bypass mode are provided. The elliptic filter is a 10th order low pass filter with a linear phase and a root raised cosine amplitude response. It has very steep roll-off and its cutoff frequency is programmable from 1.6 KHz to 104 KHz. The Bessel filter is an 8th order low pass filter with a linear phase response over its entire passband. It exhibits little to no over-shoot, under-shoot, or ringing with pulse type signals and its cutoff frequency can be programmed from 300Hz to 88 KHz. If desired, the filters can be bypass. In the case, only a fixed $2^{nd}$ order active RC low pass filter with a cutoff frequency of around 400 KHz is provided.

### 3.1.6 Programmable Gain Amplifier (PGA)

The programmable gain amplifier (PGA) provides a programmable (back-end) gain of 1, 2, 5, 10, 20, 50, and 100.

### 3.1.7 Analog Digital Converter (ADC)

The ADC converts the analog input signal to a digital value. The ADC is a 14-bit that uses successive approximation register (SAR) architecture with no pipeline delay to perform the analog-to-digital conversion.

### 3.1.8 Aperture Comparator

The aperture comparator logic provides real-time data compression of the input signal. The aperture comparator logic compares the new data value with the last stored value to provide a real-time decision to store or not store the data. Various aperture modes allow easy storage of only the desired data reducing storage and data transfer requirements. Two programmable apertures (A & B) each with a high and low value allow flexible setting of the desired data. Depending on the aperture mode, the logic can use an external signal switch between the two apertures or automatically switch.

### 3.1.9 FIFO

The synchronous read/write first-in first-out (FIFO*) memory provides data storage for up to 32 million value-time pairs or 64 million A/D values. In value-time pair storage mode, the value-time pairs are stored as 48-bit wide data and retrieved by the user as a three 16-bit word set or as a two 32-bit word set. In value storage only mode, the A/D value is stored in the upper 32-bits of memory and retrieved by the user as a single 16-bit words or as a 32-bit word sets.

* Note: Although the memory is technically a FIFO, a random access capability is provided to allow the read pointer to be positioned at any point in memory. This capability is very useful in continuous capture mode where the data of interest may be near the end of the FIFO.

### 3.1.10 32-Bit Timestamp

The 32-bit timer provides a time stamp of the data stored. The time increments by one on each rising edge of the sample clock. The timer can be reset independent of the A/D conversion enable or at the same time and can be programmed to continue running while A/D conversion is disabled. Over one hour of uniquely time-stamped data can be captured when running a sample rate of 1M samples per second. A timestamp rollover interrupt allows unique time stamping for an indefinite amount of time.

### 3.1.11 Clock/Run Control

This logic provides selection and control of the sample clock and timestamp run enable signals. These signals can be generated internally or provided by an external source through the front panel or backplane triggers. The logic includes a prescaler that can divide the input clock frequency by a value from 1 to 100,000 to produce the desired sample rate. In addition, the sample clock and timestamp run enable signals can be output to the front panel connector or to the backplane triggers to serve as the master control for multiple M228's in a system.

### 3.1.12 On-board Oscillator

An on-board oscillator provides a base 1MHz to the clock control logic. This oscillator can be used to perform the A/D conversion and time stamping.

### 3.1.13 External Inputs and Control

Two front panel inputs are provided for external control of the sample clock rate, A/D conversion enable, and other signals. Each input has a programmable threshold level, input impedance, and logic inversion capability. In addition, the signals can be internally latched to provide a typical armed, ready, triggered function.

### 3.1.14 External Outputs and Control

Two front panel outputs are provided for external synchronization of other system components. A variety of internal signals can be routed to the front panel outputs.

### 3.1.15 M-Triggers & Control

Two bidirectional backplane triggers (TRIGA/B) allow control the sample clock rate, A/D conversion enable, and other signals through a carrier or system backplane. In addition, a variety of internal signals can be routed and output to the backplane trigger system.

### 3.1.16 Calibration

Calibration is provided through an on-board digital potentiometer that allows adjustment of the 0V offset and full scale reading. Calibration can be performed using on-board references or at a system level using external references. Calibration values are stored in an on-board non-volatile EEPROM.

## 3.2 INPUT/OUTPUT SIGNALS

The front panel I/O connector is a standard 44-pin D-subminiature female receptacle (CONEC P/N 164A18119X or equivalent). Below are the signals and functional descriptions provided on the connector (see Appendix A for pin assignments).

| | |
|---|---|
| AIN+/- | Differential Analog Input Signals |
| FPINA/B | Front Panel Input A & B. These contacts can be used to input an external sample clock, A/D conversion enable, or RUN enable signal (Input threshold is programmable from 0V to +5.0V, input impedance is programmable for Hi-Z or 50 Ω). |
| FPOUTA/B | Front Panel Output A & B. These contacts can be programmed to output the master sample clock, A/D conversion enable, or run enable signal (TTL output levels). |
| AUX+5V | Auxiliary +5V power for an external buffer, amplifier, or other logic. *(Do not exceed 500mA)* |
| AUX+12V | Auxiliary +12V power for an external buffer, amplifier, or other logic. *(Do not exceed 100mA)* |
| AUX-12V | Auxiliary -12V power for an external buffer, amplifier, or other logic. *(Do not exceed 100mA)* |
| GND | Ground (common ground for the FPINA/B, FPOUTA/B, AUX+5V, AUX+12V, and AUX-12V). |

## 3.3 CONFIGURATION AND IDENTIFICATION

### 3.3.1 Programming Registers

There are a variety of registers used to configure and control the M228 module. These registers are located as an offset from the base address of the module. The absolute address depends on the M-module carrier for which the M228 is installed. See the carrier's User Manual for details. The address map and details of the registers are shown in Table I and Figure 9.

**Table I. Register Address Map**

| IO REG. (HEX) | 32-Bit | REGISTER DESCRIPTION |
|---|---|---|
| 00 | * | ID |
| 02 | | Revision |
| 04 | * | Master Control |
| 06 | | Interrupt Control |
| 08 | * | Function Source Control |
| 0A | | Clock Control |
| 0C | * | Output Source Map |
| OE | | (reserved) |
| 10 | * | Input A Control |
| 12 | | Input B Control |
| 14 | * | Aperture High A |
| 16 | | Aperture Low A |
| 18 | * | Aperture High B |
| 1A | | Aperture Low B |
| 1C-1E | | (reserved) |
| 20 | * | FIFO Data Port (32-bit/16-bit) |
| 22 | | (reserved) |
| 24 | * | FIFO Unread Count (High) |
| 26 | | FIFO Unread Count (Low) |
| 28 | * | Last Value Stored |
| 2A | | Current Value |
| 2C | * | Time Stamp (High) |
| 2E | | Time Stamp (Low) |
| 30 | * | Peripheral Variable Voltage |
| 32 | | (reserved) |
| 34 | * | Random Data Port (32-bit/16-bit) |
| 36 | | (reserved) |
| 38 | * | Random Data Address (High) |
| 3A | | Random Data Address (Low) |
| 3A-3E | | (reserved) |
| 40 | * | Analog Input Control |
| 42 | | Anti-Aliasing Filter Control |
| 44 | * | A/D Temperature |
| 46 | | Calibration Fullscale/Offset |
| 48 | * | Calibration EEPROM Control |
| 4A | | Calibration EEPROM Data |
| 4C-FC | | (reserved) |
| FE | | IDPROM |

Note: The * indicates allowable 32-bit access boundaries.

Reg 00

## ID Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read only) | | | | | | | | (read only) | | | | | | | |
| Read | CONFIG | | | | | | | | MODEL | | | | | | | |

CONFIG ⇨ Configuration Number (dash number of the unit according to the following table)
0 Normal
Others Undefined
MODEL ⇨ Model Number (always reads hex E4, decimal 228)

Reg 02

## Revision Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read only) | | | | | | | | (read only) | | | | | | | |
| Read | RESERVED | | | | | | | | LGMAJ | | | | LGMIN | | | |

LGMAJ ⇨ Logic Major Revision (first major release is 1, prerelease is 0)
LGMIN ⇨ Logic Minor Revision (minor releases involve insignificant changes or corrections)
RESERVED ⇨ Reserved (this value should be ignored, it is reserved for special information)



**Figure 9. Programming Registers**

Reg 04

## Master Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | - | - | CTSR | CCM | RFF | RTS | STM | | - | - | FST | ASEL | ACE | TRUN |
| Read | FF | HF | QF | NE | TSR | CCM | 0 | 0 | STM | | 0 | 0 | FST | ASEL | ACE | TRUN |

FF ⇨ FIFO Full (1 = full) [1]
HF ⇨ FIFO Half Full (1 = FIFO is at least half full)
QF ⇨ FIFO Quarter Full (1 = FIFO is at least one quarter full)
NE ⇨ FIFO Not Empty (1 = FIFO has at least one time-value pair stored)
TSR ⇨ Time Stamp Rollover (1 = Time Stamp Rollover occurred)
CTSR ⇨ Clear Time Stamp Rollover (1 = Clear Time Stamp Rollover status)
CCM ⇨ Continuous Capture Mode [2] (0 = stop capturing data when FIFO is full (CTF Mode), 1 = continuously capture data even when FIFO is full (CCM))
RFF ⇨ Reset FIFO (1 = reset)
RTS ⇨ Reset Time Stamp Counter (1 = reset)
STM ⇨ Storage Mode
- 00 normal value-time pair storage
- 01 value storage only
- 10 (reserved)
- 11 no storage

FST ⇨ Force Store (0 = normal operation, 1 = force the storage of any value ignoring aperture values) [3]
ASEL ⇨ Aperture Select (0 = use "A" aperture values, 1 = use "B" aperture values) [3]
ACE ⇨ A/D Conversion Enable (0 = disable, 1 = enable) [3, 4]
TRUN ⇨ Timestamp Run (0 = timestamp clock disabled, 1 = timestamp clock enabled) [3]

Notes:
1. In CTF mode, FIFO Full is an error condition and capturing of data stops. In CCM, FIFO Full is only an indicator.
2. See 4.2 for details on operation in these modes.
3. The FST, ASEL, ACE and TRUN bits only set the software value for the control. The source of the function must be defined as "Software Register" in the Function Source Control and Clock Control Registers to use these bits.
4. When STM = 00, value-time storage can only occur when ACE is enabled. If ACE is disabled and TRUN is enabled, the timestamp counter will run, but no data will be stored.

**Figure 9. Programming Registers (continued)**

Reg 06

## Interrupt Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | FFIP | HFIP | QFIP | NEIP | TSRP | - | - | - | FFIE | HFIE | QFIE | NEIE | TSRE | - | - | GIE |
| Read | FFIP | HFIP | QFIP | NEIP | TSRP | 0 | 0 | 0 | FFIE | HFIE | QFIE | NEIE | TSRE | 0 | 0 | GIE |

FFIP ⇨ FIFO Full Interrupt Pending (1 = pending) [1]
HFIP ⇨ FIFO Half Full Interrupt Pending (1 = pending) [1]
QFIP ⇨ FIFO One-Quarter Full Interrupt Pending (1 = pending) [1]
NEIP ⇨ FIFO Not Empty Interrupt Pending (1= pending) [1]
TSRP ⇨ Time Stamp Rollover Interrupt Pending (1 = pending) [1]
FFIE ⇨ FIFO Full Interrupt Enable (1 = enable)
HFIE ⇨ FIFO Half Full Interrupt Enable (1 = enable)
QFIE ⇨ FIFO One-Quarter Full Interrupt Enable (1 = enable)
NEIE ⇨ FIFO Not Empty Interrupt Enable (1 = enable)
TSRE ⇨ Time Stamp Rollover Interrupt Enable (1 = enable)
GIE ⇨ Global Interrupt Enable (1 = enable) [2]

Notes:
1. To clear a pending interrupt, writing a '1' to the interrupt pending bit.
2. GIE bit is automatically cleared when an interrupt acknowledge is received. Software must re-enable GIE after servicing the interrupt to receive further interrupts.
3. During an interrupt acknowledge (IACK) cycle, the upper byte of this register is presented as the interrupt vector.



**Figure 9. Programming Registers (continued)**

Reg 08

## Function Source Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | FSL | FSTSRC | | | ASL | ASELSRC | | | ACL | ACESRC | | | TRL | TRUNSRC | | |
| Read | FSL | FSTSRC | | | ASL | ASELSRC | | | ACL | ACESRC | | | TRL | TRUNSRC | | |

FSL ⇨ Force Store All Active Level (0 = active high, 1 = active low)

FSTSRC ⇨ Force Store All Source

| | | | |
|---|---|---|---|
| 000 | Software Register (FACQ bit) | 100 | Backplane Trigger A |
| 001 | (reserved) | 101 | Backplane Trigger B |
| 010 | FPINA signal | 110 | (reserved) |
| 011 | FPINB signal | 111 | (reserved) |

ASL ⇨ Aperture Select Active Level (0 = active high, 1 = active low)

ASELSRC ⇨ Aperture Select Source

| | | | |
|---|---|---|---|
| 000 | Software Register (ASEL bit) | 100 | Backplane Trigger A |
| 001 | (reserved) | 101 | Backplane Trigger B |
| 010 | FPINA signal | 110 | (reserved) |
| 011 | FPINB signal | 111 | (reserved) |

ACL ⇨ A/D Conversion Enable Active Level (0 = active high, 1 = active low)

ACESRC ⇨ A/D Conversion Enable Source

| | | | |
|---|---|---|---|
| 000 | Software Register (ACE bit) | 100 | Backplane Trigger A |
| 001 | (reserved) | 101 | Backplane Trigger B |
| 010 | FPINA signal | 110 | (reserved) |
| 011 | FPINB signal | 111 | (reserved) |

TRL ⇨ Timestamp Run Enable Active Level (0 = active high, 1 = active low)

TRUNSRC ⇨ Timestamp Run Enable Source

| | | | |
|---|---|---|---|
| 000 | Software Register (RUN bit) | 100 | Backplane Trigger A |
| 001 | (reserved) | 101 | Backplane Trigger B |
| 010 | FPINA signal | 110 | (reserved) |
| 011 | FPINB signal | 111 | (reserved) |



**Figure 9. Programming Registers (continued)**

Reg 0A

## Clock/Aperture Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | SCLK | - | - | - | - | APMODE | | | PSC | | | | - | CLKSRC | | |
| Read | 0 | 0 | 0 | 0 | 0 | APMODE | | | PSC | | | | 0 | CLKSRC | | |

SCLK ⇨ Software Clock (1 = toggles sample clock high then low) [1, 2]

APMODE ⇨ Aperture Mode

0 Store if outside selected aperture window
1 Store once outside selected “absolute” window and outside of aperture window "B" [3]
2 Store if outside absolute window "A" and outside of aperture window "B"
3 Store once inside selected absolute window and outside of aperture window "B" [3]
4 Store if inside absolute window "A" and outside of aperture window "B"
5 Store if outside both absolute window "A" and "B"
6 Store if inside either absolute window "A" or "B"
7 (reserved)

PSC ⇨ Prescaler Control (Selected clock is divided by this prescaler)

| Value | Prescaler | Value | Prescaler | Value | Prescaler | Value | Prescaler |
|---|---|---|---|---|---|---|---|
| 0000 | 1 | 0100 | 20 | 1000 | 500 | 1100 | 10000 |
| 0001 | 2 | 0101 | 50 | 1001 | 1000 | 1101 | 20000 |
| 0010 | 5 | 0110 | 100 | 1010 | 2000 | 1110 | 50000 |
| 0011 | 10 | 0111 | 200 | 1011 | 5000 | 1111 | 100000 |

CLKSRC ⇨ Clock Source

| | | | |
|---|---|---|---|
| 000 | Internal Oscillator | 100 | Backplane Trigger A |
| 001 | Software Register (SCLK bit) | 101 | Backplane Trigger B |
| 010 | FPINA signal | 110 | (reserved) |
| 011 | FPINB signal | 111 | (reserved) |

Notes:

1. The Clock Source (CLKSRC) field must first be specified as “Software Register” before writing a ‘1’ to the SCLK bit.
2. Writing a ‘1’ to SCLK field, produces an internal high then low pulse.
3. Once the signal crosses outside (or inside) the absolute window “A” the aperture window “B” is used. A Reset FIFO (RFF) is required to use aperture “A” again.

Reg 0C

## Output Source Map Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | ITOB | TBSRC | | | ITOA | TASRC | | | IFOB | FBSRC | | | IOFA | FASRC | | |
| Read | ITOB | TBSRC | | | ITOA | TASRC | | | IFOB | FBSRC | | | IOFA | FASRC | | |

ITOA/ITOB ⇨ Invert Trigger Output

TASRC/TBSRC ⇨ Trigger Output Source

| | | | |
|---|---|---|---|
| 0 | Disabled (input) | 4 | Aperture Select Signal |
| 1 | Sample Clock (after prescaler) | 5 | A/D Conversion Enable Signal |
| 2 | Clock (before prescaler) | 6 | Timestamp Run Enable Signal |
| 3 | Force Store Signal | 7 | Value Stored Strobe |

IFOA/IFOB ⇨ Invert Front Panel Output

FASRC/FBSRC ⇨ Front Panel Output Source

| | | | |
|---|---|---|---|
| 0 | Disabled (High-Z) | 4 | Aperture Select Signal |
| 1 | Sample Clock (after prescaler) | 5 | A/D Conversion Enable Signal |
| 2 | Clock (before prescaler) | 6 | Timestamp Run Enable Signal |
| 3 | Force Store Signal | 7 | Value Stored Strobe |

**Figure 9. Programming Registers (continued)**

Reg 10

## Input A Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | CLTA | CLFA | - | IIFA | IVTA | IVFA | LTA | LFA | Input Threshold FP A (ITFA) | | | | | | | |
| Read | TAS | FAS | 0 | IIFA | IVTA | IVFA | LTA | LFA | Input Threshold FP A (ITFA) | | | | | | | |

CLTA ⇨ Clear Latched TRIGINA (1 = clears latched signal) [1]
CLFA ⇨ Clear Latched FPINA (1 = clears latched signal) [1]
TAS ⇨ TRIGINA Status (0 = low, 1 = high, after inversion and latching)
FAS ⇨ FPINA Status (0 = low, 1 = high, after inversion and latching)
IIFA ⇨ FPINA Input Impedance (0 = Hi-Z, 1 = 50Ω)
IVTA ⇨ Invert TRIGINA Input (0 = normal, 1 = invert)
IVFA ⇨ Invert FPINA (0 = normal, 1 = invert)
LTA ⇨ Latch TRIGINA Input (0 = no latching, 1 = latch on rising edge) [2]
LFA ⇨ Latch FPINA (0 = no latching, 1 = latch on rising edge) [2]
ITFA ⇨ Input Threshold Level of FPINA ($00_{16}$ = 0V (default), $FF_{16}$ = +5V)

Notes:
1. The latched value is cleared by writing a '1' to the CLTA or CLFA bit.
2. Latching occurs on the rising edge of the signal after inversion, if specified.

Reg 12

## Input B Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | CLTB | CLFB | - | IIFB | IVTB | IVFB | LTB | LFB | Input Threshold FP B (ITFB) | | | | | | | |
| Read | TBS | FBS | 0 | IIFB | IVTB | IVFB | LTB | LFB | Input Threshold FP B (ITFB) | | | | | | | |

CLTB ⇨ Clear Latched TRIGINB (1 = clears latched signal) [1]
CLFB ⇨ Clear Latched FPINB (1 = clears latched signal) [1]
TBS ⇨ TRIGINB Status (0 = low, 1 = high, after inversion and latching)
FBS ⇨ FPINB Status (0 = low, 1 = high, after inversion and latching)
IVTB ⇨ Invert TRIGINB Input (0 = normal, 1 = invert)
IIFB ⇨ FPINB Input Impedance (0 = Hi-Z, 1 = 50Ω)
IVFB ⇨ Invert FPINB (0 = normal, 1 = invert)
LTB ⇨ Latch TRIGINB Input (0 = no latching, 1 = latch on rising edge) [2]
LFB ⇨ Latch FPINB (0 = no latching, 1 = latch on rising edge) [2]
ITFB ⇨ Input Threshold Level of FPINB ($00_{16}$ = 0V (default), $FF_{16}$ = +5V)

Notes:
1. The latched value is cleared by writing a '1' to the CLTB or CLFB bit.
2. Latching occurs on the rising edge of the signal after inversion, if specified.

**Figure 9. Programming Registers (continued)**

Reg 14

## Aperture High A Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | Aperture High A Value | | | | | | | | | | | | | |
| Read | 0 | 0 | Aperture High A Value | | | | | | | | | | | | | |

Aperture High A ⇨ This value is used to determine if the A/D value is stored to memory. The storage criterion depends on the Aperture Mode.

Note: See note below.

Reg 16

## Aperture Low A Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | Aperture Low A Value | | | | | | | | | | | | | |
| Read | 0 | 0 | Aperture Low A Value | | | | | | | | | | | | | |

Aperture Low A ⇨ This value is used to determine if the A/D value is stored to memory. The storage criterion depends on the Aperture Mode.

Note: See note below.

Reg 18

## Aperture High B Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | Aperture High B Value | | | | | | | | | | | | | |
| Read | 0 | 0 | Aperture High B Value | | | | | | | | | | | | | |

Aperture High B ⇨ This value is used to determine if the A/D value is stored to memory. The storage criterion depends on the Aperture Mode

Note: See note below.

Reg 1A

## Aperture Low B Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | Aperture Low B Value | | | | | | | | | | | | | |
| Read | 0 | 0 | Aperture Low B Value | | | | | | | | | | | | | |

Aperture Low B ⇨ This value is used to determine if the A/D value is stored to memory. The storage criterion depends on the Aperture Mode.

Note: Aperture values are always specified as two's complement numbers, which represent both positive and negative values. When specifying an aperture window (versus a fixed window), the user must ensure that only positive values are specified.

**Figure 9. Programming Registers (continued)**

Reg 20
(32-bit)

## FIFO Data Port Register

| Bit | 31 | 30 | 16 | 15 | 0 |
|---|---|---|---|---|---|
| Read 1 | DV | RERR | A/D Data Value | All 0's | |
| Read 2 | Time Stamp [3] | | | | |

Reg 20
(16-bit)

## FIFO Data Port Register [1]

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read 1 | DV | 0 | A/D Data Value | | | | | | | | | | | | | |
| Read 2 | Time Stamp (upper half) [3] | | | | | | | | | | | | | | | |
| Read 3 | Time Stamp (lower half) [3] | | | | | | | | | | | | | | | |

DV ⇨ Data Valid (1 = valid data, 0 = FIFO empty) [2]
RERR ⇨ Read Error (1 = an error occurred reading the FIFO memory)
A/D Data Value ⇨ 14-bit A/D value
Time Stamp ⇨ 32-bit Time Stamp [3]

Notes:
1. 8-bit register reads of the FIFO Data Port Register are not supported.
2. Read 2 (and Read 3) data are only returned if Read 1 data indicates a valid data entry (DV = 1).
3. In Value Storage Only mode (STM = 1), all reads represent an A/D Data Value. The DV bit indicates validity of the data. On 32-bit reads, both upper and lower 16-bits contain an A/D Data Value.

Reg 24

## FIFO Unread Count Register (High)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | 0 | 0 | 0 | 0 | 0 | 0 | Count (D25-D16) | | | | | | | | | |

Reg 26

## FIFO Unread Count Register (Low)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | Count (D15-0) | | | | | | | | | | | | | | | |

Count ⇨ Number of time-value pairs that have not been read by the user.

Notes:
1. To guarantee consistency between the High and Low registers when reading as 16-bit words, the High register must be read first. Internally, the Low register is latched when the High register is read.
2. In Value Storage Only mode (STM = 1), the FIFO is treated as 16 bits wide; therefore, the unread count represents one data entry.

**Figure 9. Programming Registers (continued)**

Reg 28

## Last Value Stored Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | 0 | 0 | Last Stored | | | | | | | | | | | | | |

Last Stored ⇨ Last A/D value stored in FIFO

Reg 2A

## Current Value Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | 0 | 0 | Current Value | | | | | | | | | | | | | |

Current Value ⇨ Current (Last) value read from A/D

Note: This register is updated after every A/D conversion; therefore, A/D conversion must be enabled and sample clock must be present.

Reg 2C

## Time Stamp Register (High)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | Time Stamp (D31-D16) | | | | | | | | | | | | | | | |

Reg 2E

## Time Stamp Register (Low)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | (read-only) | | | | | | | | | | | | | | | |
| Read | Time Stamp (D15-0) | | | | | | | | | | | | | | | |

Time Stamp ⇨ Snapshot of current Time Stamp value.

Note: To guarantee consistency between the High and Low registers when reading as 16-bit words, the High register must be read first. Internally, the Low register is latched when the High register is read.

Reg 30

## Peripheral Variable Voltage Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | - | - | PVARV | | | | | | | | | | | |
| Read | 0 | 0 | 0 | 0 | PVARV | | | | | | | | | | | |

PVARV ⇨ Peripheral Variable Voltage Level ($000_{16}$ = -10V (default), $800_{16}$ = 0V, $FFF_{16}$ = +10V)

**Figure 9. Programming Registers (continued)**

Reg 34
(32-bit)

## Random Data Port Register

| Bit | 31 | 30 | 16 | 15 | 0 |
|---|---|---|---|---|---|
| Read 1 | DV | RERR | A/D Data Value | All 0's | |
| Read 2 | Time Stamp [3] | | | | |

Reg 34
(16-bit)

## Random Data Port Register [1]

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read 1 | DV | 0 | A/D Data Value | | | | | | | | | | | | | |
| Read 2 | Time Stamp (upper half) [3] | | | | | | | | | | | | | | | |
| Read 3 | Time Stamp (lower half) [3] | | | | | | | | | | | | | | | |

DV ⇨ Data Valid (1 = valid data, 0 = FIFO empty) [2]
RERR ⇨ Read Error (1 = an error occurred reading the FIFO memory)
A/D Data Value ⇨ 14-bit A/D value
Time Stamp ⇨ 32-bit Time Stamp [3]

Notes:
1. 8-bit register reads of the Random Data Port Register are not supported.
2. Read 2 (and Read 3) data are only returned if Read 1 data indicates a valid data entry (DV = 1).
3. In Value Storage Only mode (STM = 1), all reads represent an A/D Data Value. The DV bit indicates validity of the data. On 32-bit reads, both upper and lower 16-bits contain an A/D Data Value.
4 Reading this register does not change the FIFO Unread Count.

Reg 38

## Random Data Address Register (High)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | | | | | | | | | | | | | | | | |
| Read | 0 | 0 | 0 | 0 | 0 | 0 | RADDR (D25-D16) | | | | | | | | | |

Reg 3A

## Random Data Address Register (Low)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | | | | | | | | | | | | | | | | |
| Read | RADDR (D15-0) | | | | | | | | | | | | | | | |

RADDR ⇨ FIFO Memory Address to access when the Random Data Port Register is read

Notes:
1. To guarantee consistency between the High and Low registers when reading as 16-bit words, the High register must be read first. Internally, the Low register is latched when the High register is read.
2. In Value Storage Only mode (STM = 1), the FIFO is treated as 16 bits wide; therefore, the unread count represents one data entry.
3. This register automatically increments each time the Random Data Port Register is read.

**Figure 9. Programming Registers (continued)**

Reg 40

## Analog Input Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | REFE | REFSEL | | | SIM | | FT | WARP | IVDD | - | FGAIN | | - | BGAIN | | |
| Read | REFE | REFSEL | | | SIM | | FT | WARP | IVDD | 0 | FGAIN | | 0 | BGAIN | | |

REFE ⇨ Reference Enable (0 = normal operation, 1 = enable reference signal injection)

REFSEL ⇨ Reference Select

- 0 Ground (0V)
- 1 0.5V
- 2 -0.5V
- 3 10V
- 4 -10V
- 5 Variable [1]
- 6 +5V Supply [1]
- 7 +3.3V Supply [1]

SIM ⇨ Simulation Mode (non-zero = simulate a full scale triangle waveform input) [2]

- 0 Normal Mode
- 1 Count Up from midpoint
- 2 Count Down from midpoint
- 3 (reserved)

FT ⇨ Factory Test (0 = normal operation, 1 = factory test mode) [3]

WARP ⇨ Warp Mode (0 = normal mode (≤800KSPS), 1 = fast conversion rate mode (>800KSPS) [4]

IVDD ⇨ Input Voltage Divider Disable (0 = enabled - 10:1(default), 1 = disabled - 1:1)

FGAIN ⇨ Front End Gain

- 0 G = 1
- 1 G = 2
- 2 G = 5
- 3 G = 10

BGAIN ⇨ Back End Gain

- 0 G = 1
- 1 G = 2
- 2 G = 5
- 3 G = 10
- 4 G = 20
- 5 G = 50
- 6 G = 100
- 7 G = 0 (disables output)

Notes:

1. The variable voltage (PVARV), +5V Supply, and +3.3V Supply can be used to perform general self test functions. They should NOT be used to perform calibration. The PVARV level is controlled using the Peripheral Variable Voltage Register (Reg 26).
2. The simulation mode can be used to verify internal operation of the memory, control and aperture logic. In this mode, full scale triangle wave data is simulated and returned at the sample clock rate.
3. In Factory Test mode, the upper 16-bits of the Timestamp equal the 1's complement of the lower sixteen bits.
4. For sample frequencies >800KSPS, the A/D must be set to Warp Mode. See 4.1 for details about the A/D behavior in this mode.

**Figure 9. Programming Registers (continued)**

Reg 42

## Anti-Aliasing Filter Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | - | - | FCUTOFF | | | | - | - | - | - | - | - | FSEL | |
| Read | 0 | 0 | 0 | 0 | FCUTOFF | | | | 0 | 0 | 0 | 0 | 0 | 0 | FSEL | |

FCUTOFF ⇨ Filter Cutoff Frequency

| Value | Elliptic | Bessel |
|---|---|---|
| 0 | 1.6KHz | 300Hz |
| 1 | 3.2KHz | 600Hz |
| 2 | 6.5KHz | 1.4KHz |
| 3 | 13KHz | 2.8 KHz |
| 4 | 26KHz | 5.5 KHz |
| 5 | 52KHz | 11 KHz |
| 6 | 104KHz | 22 KHz |
| 7 | Invalid | 44 KHz |
| 8 | Invalid | 88 KHz |
| 9-15 | Invalid | Invalid |

FSEL ⇨ Filter Type Select

| | |
|---|---|
| 0 | Bypass [1] |
| 1 | Elliptic |
| 2 | Bessel |
| 3 | invalid |

Note: When Bypass is selected, the elliptic and Bessel filters are bypassed; however, a fixed 2nd order active RC filter with a cutoff frequency of 400 KHz is still in place to eliminate unwanted high frequency signals.

Reg 44

## A/D Temperature Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | DTR | - | - | - | - | - | - | (read-only) | | | | | | | | |
| Read | DTR | 0 | 0 | 0 | 0 | 0 | NEGT | ADTEMP | | | | | | | | |

DTR ⇨ Disable Temperature Read (1 = disable temperature reading) [1]

NEGT ⇨ Negative Temperature (1 = the temperature is below zero)

ADTEMP ⇨ A/D Temperature Value

| NEGT | Temperature Formula |
|---|---|
| 0 | ADTEMP ÷ 4 |
| 1 | (ADTEMP - 512) ÷ 4 |

Note: Reading of the A/D board temperature is performed every 0.5 seconds through a serial bus protocol. The DTR bit is provided to allow this automatic operation to be disabled for cases where noise reduction is crucial.

**Figure 9. Programming Registers (continued)**

Reg. 46

## Calibration Fullscale/Offset Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | FSVAL | | | | | | | | OSVAL | | | | | | | |
| Read | FSVAL | | | | | | | | OSVAL | | | | | | | |

FSVAL ⇨ Full-scale Calibration Value (default = 0x80)
OSVAL ⇨ Offset Calibration Value (default = 0x80)

Notes:

1. This register controls digital potentiometers that do not retain their settings when powered off. Application driver software must initialize the calibration potentiometers before using the A/D converter.
2. Data is automatically read-back from the calibration potentiometers after reset/initialization and after a write to this register.
3. The OPC flag in the Calibration EEPROM Control Register goes low when the write operation is started and high when the data write and read-back operations are complete.

Reg. 48

## Calibration EEPROM Control Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | - | - | WPR | RPR | - | - | - | ADDR | | | | | | | | - |
| Read | OPC | IERR | 0 | 0 | 0 | 0 | 0 | ADDR | | | | | | | | 0 |

OPC ⇨ Operation Complete (0 = working, 1 = done) [1]
IERR ⇨ Internal Bus (I2C) Error (1 = an error occurred) [2]
WPR ⇨ Write EEPROM Value (1 = write) [3]
RPR ⇨ Read EEPROM Value (1 = read) [4]
WADDR ⇨ Set EEPROM Write Address (address is word aligned)

Notes:

1. The OPC flag goes low when an operation is started and high when the operation is complete. Software must always check the OPC flag before attempting an operation. See special note for EEPROM write operations.
2. This bit indicates an error occurred on the last internal I2C bus operation, which is used for the EEPROM, Full Scale & Offset adjust, A/D temperature reading, and reference select operations.
3. When a 1 is written to the WPR bit, the EEDATA in the Calibration EEPROM Data Register is written to the EEPROM address specified in the ADDR field. Allow an additional 5ms after the OPC flag before performing another EEPROM operation.
4. When a 1 is written to RPR bit, the data at location ADDR is read and placed in the Calibration EEPROM Data Register. The OPC will go high when the read is complete and the EEDATA value is valid.

**Figure 9. Programming Registers (continued)**

Reg. 4A

## Calibration EEPROM Data Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | EEDATA | | | | | | | | | | | | | | | |
| Read | EEDATA | | | | | | | | | | | | | | | |

Notes:

1. A read/write is performed from/to the address in the ADDR field in the Calibration EEPROM Control Register.
2. The OPC flag in the Calibration EEPROM Control Register goes low when an operation is started and high when the operation is complete. Software must always check the OPC flag before attempting an operation. Write operations can take up to 5ms to complete. Read operations complete in less than 1ms.

Reg. FE

## IDPROM Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write | Not Used | | | | | | | | | | | | | CS | CLK | DIO |
| Read | 0 | | | | | | | | | | | | | CS | CLK | DIO |

CS ⇨ IDPROM Chip Select
CLK ⇨ IDPROM Clock
DIO ⇨ IDPROM Data Input/Output

Note: See 3.3.2 for details on using this register.

**Figure 9. Programming Registers (continued)**

### 3.3.2 M-Module Identification PROM

The M228 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (0xFE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.6.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

**Table II. M-Module EEPROM IDENT Words**

| Word | Description | Value (hex) |
|---|---|---|
| 0 | Sync Code | 5346 |
| 1 | Module Number | 00E4 (228 dec.) |
| 2 | Revision Number [1] | 1010 |
| 3 | Module Characteristics [2] | 1E70 |
| 4-7 | Reserved | 0000 |
| 8-15 | M-Module Specific | 0000 |
| 16 | VXI Sync Code | ACBA |
| 17 | VXI ID | 0FC1 (C&H) |
| 18 | VXI Device Type [3] | FFD4 |
| 19-31 | Reserved | 0000 |
| 32-63 | M-Module Specific | 0000 |

Notes:

1) The Revision Number is the logic firmware and hardware functional revision level of the module. The hardware revision number does not necessarily correspond to the hardware assembly level. The bits definitions are:

| Bit(s) | Description |
|---|---|
| 15-12 | Software Major Revision (1.0 is first major release) |
| 11-8 | Software Minor Revision |
| 7-4 | Hardware Major Revision (1.0 is first major release) |
| 3-0 | Hardware Minor Revision |

2) The Module Characteristics bit definitions are:

| Bit(s) | Description | Bit(s) | Description |
|---|---|---|---|
| 15 | 0 = no burst access | 8/7 | 00 = no DMA requestor |
| 14/13 | Unused | 6/5 | 11 = INTC (INTB also supported) |
| 12 | 1 = module needs ±12V | 4/3 | 10 = 32-bit data |
| 11 | 1 = module needs +5V | 2/1 | 00 = 8-bit address bus |
| 10 | 1 = trigger outputs supported | 0 | 0 = no memory access |
| 9 | 1 = trigger inputs supported | | |

3) The VXI Device Type word contains the following information:

| Bit(s) | Description |
|---|---|
| 15-12 | $F_{16}$ = 256 bytes of required memory |
| 11-0 | $FD4_{16}$ = C&H specified VXI model code for M228 |

## 4.0 OPERATION

The M228 is a register-based instrument that is controlled through a series of registers described in Section 3.3.1. A high-level software driver is available to aid in programming of the module.

### 4.1 A/D CONVERSION

The M228 uses a fast, low power, precision, 14-bit analog-to-digital converter (ADC) that use a successive approximation capacitive digital-to-analog (CDAC) converter architecture that has no pipeline delay. The M228 uses two of the ADC's conversion modes for operation. In Normal Mode, the ADC is capable of performing conversions at a throughput rate up to 800KSPS and has no limitation on the time between conversions. In Warp mode, the specified accuracy is only guaranteed if the time between conversions is less than 1ms. If the time between two consecutive conversions exceeds 1ms, the first conversion result should be ignored. In Warp mode, the ADC performs a background calibration during the conversion process. This calibration can drift if the time between conversions exceeds 1ms causing the first conversion to appear offset.

### 4.2 VALUE-TIME PAIR STORAGE

When and how the 14-Bit A/D Data Value and 32-Bit Timestamp are stored in the FIFO memory depends on a number of factors. These factors include the Continuous Capture Mode (CCM), the Storage Mode (STM), the Force Store (FST) setting, the A/D Conversion Enable (ACE), the Timestamp Run (TRUN) setting, and Aperture Compare result.

In Capture-Till-Full (CTF) mode (CCM = 0), the memory is treated as a standard FIFO (i.e. First In First Out) buffer. If memory becomes full, a FIFO Full Error occurs and data capturing stops. In Continuous Capture Mode (CCM = 1), the memory is treated as a circular overwriting FIFO buffer. If memory becomes full, a FIFO Full indicator occurs but data capturing continues overwriting the oldest data. When using CCM, it is best to use the Random Data Port and Random Data Address Registers to access the memory data. Given the large size of the FIFO memory, these registers allow easy access to the desired data without having to read the entire FIFO. Although memory can be read while data is being captured and stored, it is not recommended when using CCM, because the data pointer location may be indeterminate.

The Storage Mode (STM) setting determines whether the full value-timestamp pair, just the data value, or nothing is stored in the FIFO. If all A/D data is being stored (i.e., Force Store (FST = 1) mode) and the timestamp is not important, the user can set the Storage Mode (STM) in the Master Control Register to "Value Storage Only" mode. In this mode, twice as much memory is available for data.

If A/D conversion and data storage is enable, a value-time pair storage automatically occurs when the timestamp run is enabled, a timestamp rollover occurs, and when the timestamp run is disabled. These extra storage points can be used by software to easily determine start, rollover, and stop reference points.

## 4.3 APERTURE WINDOWS

The Aperture Windows define the criterion applied in real-time to determine whether or not to store data in the FIFO. There are two sets of aperture windows and each set has a high and a low value. How these aperture windows are used is determined by the Aperture Mode defined in the Clock/Aperture Control Register. Some modes use the aperture registers to define a minimum delta change required to store data and other modes use the registers to define an absolute level that data must be above or below to permit storage. Some modes combine the usage, by using Aperture Set A differently from Aperture Set B.

The aperture window set (A or B) used depends on the Aperture Mode and possibly the ASEL signal. Some aperture modes start off using aperture set A and automatically switch to aperture set B. Other aperture modes use the window set specified by the ASEL signal. The source of the ASEL signal is specified in the Function Source Control Register. The specified signal determines if aperture window set A or B is used. This signal can be changed in real-time, allowing dynamic control of the data stored.

### 4.3.1 Aperture Mode 0

Aperture Mode 0 “Store if outside selected aperture window”, allows the user to store data only if it changes more than a specified amount. For instance, if only signal changes greater than 200mV is positive direction and 100mV in the negative direction are important, the user can specify Aperture Mode 0 and set Aperture Set A High to 200mV and Aperture Set B to 100mV. The A/D reading will be stored if it is above the last stored value plus the programmed Aperture High value or it is below the last stored value minus the Aperture Low value, then the new data value is stored in the FIFO. In this mode, only positive aperture values can be specified.

### 4.3.2 Aperture Mode 1

Aperture Mode 1 “Store once outside selected absolute window A and outside of aperture window B”, allows the user start storing data once the signal level is outside of a specified window, in effect setting a trigger level. For example, if the user would like to store all data if the signal rises above 1V, Aperture High A would be set to 1V and Aperture Low A would be set to a large negative value. Aperture High and Low B would be set to 0V to effectively store all. Operation begins with Aperture Set A. If the signal level is outside the specified absolute aperture window, the logic stores the value and switches to Aperture Set B and delta window comparison. Operation continues with Aperture Set B until the FIFO is reset.

### 4.3.3 Aperture Mode 2

Aperture Mode 2 "Store if outside absolute window A and outside of aperture window B", allows the user only store data if the signal level is outside of a specified window level and the delta from the last value stored is greater than some amount. The mode is similar to Aperture Mode 1, except data is only stored if it is outside of the absolute window specified by Aperture Set A. For example, if the user would like to store data only if it is greater than +1V and less than -2V, Aperture High A would be set to +1V and Aperture Low A would be set to -2V. Aperture High and Low B would be set to level of signal change that is important as discussed in Aperture Mode 0.

### 4.3.4 Aperture Mode 3

Aperture Mode 3 "Store once inside selected absolute window A and outside of aperture window B", allows the user start storing data once the signal level falls inside of a specified window. This mode is very similar to Aperture Mode 1, except data storage will begin if the signal falls or rises to be within a specified window.

### 4.3.5 Aperture Mode 4

Aperture Mode 4 "Store if inside absolute window A and outside of aperture window B", allows the user start storing data if the signal level is inside of a specified window level. This mode is very similar to Aperture Mode 2, except data storage is stored only if the signal is inside a specified window.

### 4.3.6 Aperture Mode 5

Aperture Mode 5 "Store if outside both absolute window A and B", allows the user store all data that is outside of two absolute windows. For example, if data storage is not important when the signal is between -2V and -3V or between +4V and +8V, aperture set A would be set to -2V and -3V and aperture set B would be set to +8V and +4V. Data will be stored on every sample clock is the data level is not within on the specified windows.

### 4.3.7 Aperture Mode 6

Aperture Mode 6 "Store if inside either absolute window A and B", allows the user store all data that is inside of either absolute windows. This mode is very similar to Aperture Mode 5, except data is stored only if it is inside either window.

## 4.4 FILTER SELECTION

Two types of anti-aliasing filters and a bypass mode are provided. Using the Anti-Aliasing Filter Control Register the filter type and cutoff frequency can be selected. The elliptic filter is a 10th order low pass filter with a linear phase and a root raised cosine amplitude response. It has very steep roll-off and its cutoff frequency is programmable from 1.6 KHz to 104 KHz. The Bessel filter is an 8th order low pass filter with a linear phase response over its entire passband. It exhibits little to no over-shoot, under-shoot, or ringing with pulse type signals and its cutoff frequency can be programmed from 300Hz to 88 KHz. If desired, the filters can be bypass. In the case, only a fixed $2^{nd}$ order active RC low pass filter with a cutoff frequency of around 400 KHz is provided.

## 4.5 CALIBRATION

Calibration is provided through an on-board digital potentiometer that allows adjustment of the 0V offset and full scale reading. Calibration can be performed using on-board references or at a system level using external references. Calibration values are stored in an on-board non-volatile 512 byte EEPROM. The calibration data is stored in the EEPROM as shown in Table III and Table IV.

**Table III. EEPROM Calibration Data Format**

| Byte(s) | Description | Size | Format |
|---|---|---|---|
| 000-00E | Instrument Name | 15 bytes | M228ApertureA/D |
| 00F | Number of Entries | 1 byte | 0 - 255 |
| 010-02F | Calibration Entry 1 | 32 bytes | See Calibration Entry Table |
| 030-04F | Calibration Entry 2 | 32 bytes | " |
| 050-06F | Calibration Entry 3 | 32 bytes | " |
| 070-08F | Calibration Entry 4 | 32 bytes | " |
| 090-0AF | Calibration Entry 5 | 32 bytes | " |
| 0B0-0CF | Calibration Entry 6 | 32 bytes | " |
| 0D0-0EF | Calibration Entry 7 | 32 bytes | " |
| 0F0-10F | Calibration Entry 8 | 32 bytes | " |
| 110-12F | Calibration Entry 9 | 32 bytes | " |
| 130-14F | Calibration Entry 10 | 32 bytes | " |
| 150-16F | Calibration Entry 11 | 32 bytes | " |
| 170-18F | Calibration Entry 12 | 32 bytes | " |
| 190-1AF | Calibration Entry 13 | 32 bytes | " |
| 1B0-1CF | Calibration Entry 14 | 32 bytes | " |
| 1D0-1EF | Calibration Entry 15 | 32 bytes | " |
| 1F0-1FF | not used* | 15 bytes | " |

* Note: The last two bytes of the EEPROM are used for internal logic operation.

**Table IV. Single Calibration Entry Format**

| Byte(s) | Description | Size | Format |
|---|---|---|---|
| 00-0A | Calibration Description | 11 bytes | ASCII |
| 0B-12 | Calibration Date | 8 bytes | YYYYMMDD |
| 13-18 | Calibration Time | 6 bytes | HHMMSS |
| 19 | Calibration Temperature | 1 byte | Degrees C |
| 1A | Calibration Type | 1 byte | Internal (0, 1, 2) or External (3) |
| 1B | Front End Configuration | 1 byte | d0ff0bbb |
| 1C | Filter Configuration | 1 byte | 00ttcccc |
| 1D | Offset Cal Value | 1 byte | 0 - 255 |
| 1E | Full Scale Cal Value | 1 byte | 0 - 255 |
| 1F | | null | |

Legend: d = divider value, f = Frontend Gain, b = Backend Gain, t = filter type, c = cutoff frequency

## 4.6 ID PROM

Refer to 3.3.2 for a description of the ID PROM's function and contents. The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. Figure 10 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_eebyte (addr, id_addr);
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_eebit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_eebit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_eebit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-------------------------------------------------------------------------*/
```

*NOTE: 1. write_word and read_word are low level memory access routines.*
*2. **NOT** actual code and should be treated as a modeling tool only.*

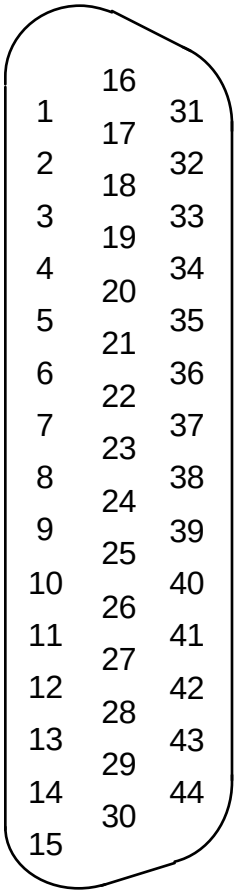
**Figure 10. ID PROM Access Routine**

# APPENDIX A: CONNECTORS

| Pin | Row A | Row B | Row C |
|---|---|---|---|
| 1 | /CS | GND | (/AS) |
| 2 | A01 | +5V | D16 |
| 3 | A02 | +12V | D17 |
| 4 | A03 | -12V | D18 |
| 5 | A04 | GND | D19 |
| 6 | A05 | (/DREQ) | D20 |
| 7 | A06 | (/DACK) | D21 |
| 8 | A07 | GND | D22 |
| 9 | D08 | D00/(A08) | TRIGA |
| 10 | D09 | D01/(A09) | TRIGB |
| 11 | D10 | D02/(A10) | D23 |
| 12 | D11 | D03/(A11) | D24 |
| 13 | D12 | D04/(A12) | D25 |
| 14 | D13 | D05/(A13) | D26 |
| 15 | D14 | D06/(A14) | D27 |
| 16 | D15 | D07/(A15) | D28 |
| 17 | /DS1 | /DS0 | D29 |
| 18 | DTACK | /WRITE | D30 |
| 19 | /IACK | /IRQ | D31 |
| 20 | /RESET | SYSCLK | /DS2 |

Note: Signals in parentheses ( ) are not used on this module.

**Figure A-1. M/MA Interface Connector Configuration**




| PIN | SIGNAL | PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|---|---|
| 1 | AIN+ | 16 | AIN– | 31 | GND |
| 2 | GND | 17 | GND | 32 | FPINA |
| 3 | | 18 | | 33 | GND |
| 4 | | 19 | | 34 | FPINB |
| 5 | | 20 | | 35 | GND |
| 6 | | 21 | | 36 | FPOUTA |
| 7 | | 22 | | 37 | GND |
| 8 | | 23 | | 38 | FPOUTB |
| 9 | | 24 | | 39 | GND |
| 10 | | 25 | | 40 | AUX+5V |
| 11 | | 26 | | 41 | GND |
| 12 | | 27 | | 42 | AUX+12V |
| 13 | | 28 | | 43 | GND |
| 14 | | 29 | | 44 | AUX-12V |
| 15 | | 30 | | | |

**Figure A-2. Front Panel Coax D-SUB Connector Configuration**

**N O T E S:**

C&H Technologies, Inc. <> 445 Round Rock West Drive <> Round Rock, TX 78681 <> www.chtech.com

## READER'S COMMENT FORM

Your comments assist us in improving the usefulness of C&H's publications; they are an important part of the inputs used for revision.

C&H Technologies, Inc. may use and distribute any of the information that you supply in any way that it believes to be appropriate without incurring any obligation whatsoever. You may, of course, continue to use the information, which you supply.

Please refrain from using this form for technical questions or for requests for additional publications; this will only delay the response. Instead, please direct your technical questions to your authorized C&H representative.

COMMENTS: _____

_____

_____

_____

_____

_____

_____

_____

Thank you for helping C&H to deliver the best possible product. Your support is appreciated.

Sincerely,

F. R. Harrison
President and CEO

**INSTRUCTIONS**

In its continuing effort to improve documentation, C&H Technologies, Inc. provides this form for use in submitting any comments or suggestions that the user may have. This form may be detached, folded along the lines indicated, taped along the loose edge (DO NOT STAPLE), and mailed. Please try to be as specific as possible and reference applicable sections of the manual or drawings if appropriate. Also, indicate if you would like an acknowledgment mailed to you stating whether or not your comments were being incorporated.

NOTE: This form may not be used to request copies of documents or to request waivers, deviations, or clarification of specification requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

——————————— (Fold along this line) ———————————

——————————— (Fold along this line) ———————————

Place Stamp Here

C&H Technologies, Inc.
Technical Publications
445 Round Rock West Drive
Round Rock, Texas 78681-5012

C&H Technologies, Inc. <> 445 Round Rock West Drive <> Round Rock, TX 78681 <> www.chtech.com