AcQuisition Technology bv

Headquarters:
Raadhuislaan 27a
5341 GL Oss

Postal address:
P.O Box 627
5340 AP Oss
The Netherlands

Phone: +31-412-651055
Fax: +31-412-651050
E-mail: info@acq.nl
Web: http://www.acq.nl

i3002

Dual M-module Carrier for 3U CompactPCI

User Manual

Version 1.0

Disclaimer:

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. AcQuisition Technology does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. AcQuisition Technology products are not designed, intended, or authorized for use as components in systems intended to support or sustain life, or for any other application in which the failure of an AcQuisition Technology product could create a situation where personal injury or death may occur, including, but not limited to AcQuisition Technology products used in defence, transportation, medical or nuclear applications. Should the buyer purchase or use AcQuisition Technology products for any such unintended or unauthorized application, the buyer shall indemnify and hold AcQuisition Technology and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that AcQuisition Technology was negligent regarding the design or manufacture of the part.

Printed in The Netherlands.

CONTENTS

1. INTRODUCTION 5
1.1. VALIDITY OF THE MANUAL 5
1.2. PURPOSE 5
1.3. SCOPE 5
1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS 5
1.5. NOTES CONCERNING THE NOMENCLATURE 5
1.6. OVERVIEW 5

2. PRODUCT OVERVIEW 7
2.1. INTRODUCTION 7
2.2. TECHNICAL OVERVIEW 7

3. INSTALLATION AND SETUP 9
3.1. UNPACKING THE HARDWARE 9
3.2. MOUNTING AN M-MODULE 9
3.3. GUIDE RAILS 10
3.4. M-MODULE INTERFACE CONNECTOR 11
3.5. COMPACTPCI INTERFACE CONNECTOR 12

4. FUNCTIONAL DESCRIPTION 15
4.1. BLOCK DIAGRAM 15
4.2. PCI TO M-MODULE BRIDGE 15
4.2.1. LOCAL BUS CONFIGURATION 16
4.2.2. INTERRUPTS. 17
4.2.3. CONFIGURATION EEPROM 17
4.3. M-MODULE INTERFACE 20
4.3.1. STANDARD ACCESSES 20
4.3.2. EXTENDED ACCESSES 21
4.3.3. BUS TIMER 21
4.3.4. TRIGGER LOGIC 22
4.4. CONTROL REGISTERS 23
4.4.1. INTERRUPT STATUS CONTROL REGISTER 23
4.4.2. TRIGGER CONTROL REGISTERS 24
4.4.3. GEOGRAPHIC ADDRESS REGISTER 27

5. SOFTWARE SUPPORT 29
5.1. APIS 29
5.2. MODSCAN 29
5.3. PXI TRIGGER LOGIC LIBRARY 29

6. ANNEX 31
6.1. BIBLIOGRAPHY 31
6.2. COMPONENT IMAGE 32
6.3. TECHNICAL DATA 33
6.4. DOCUMENT HISTORY 33

1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This is edition 1.0 of the i3002 user manual and applies to the i3002 CompactPCI M-module carrier board of revision R0.X, where 0 is the version of the PCB and X is the version of the PLD firmware.

1.2. PURPOSE

This manual serves as instruction for the operation of the i3002 M-module carrier board with CompactPCI interface. The i3002 comes with APIS based software examples, these examples are also discussed in this manual.

The i3002 is based on the PCI9030 PCI bus target interface chip of PLX Technology. For optimal performance the PCI9030 interface chip offers a wide variety of functions, a detailed description of these functions is not part of this manual. Refer to the PCI9030 data sheet for more information.

1.3. SCOPE

The scope of this manual is the usage of the i3002 - Dual M-module Carrier for 3U CompactPCI.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQuisition Platform Interface Software
CompactPCI	PCI adaption for industrial and/or embedded applications
DSP	Digital Signal Processor
ESD	Electronic Static Discharge
M-module	Mezzanine I/O concept according to the M-module specification
PCI	Peripheral Component Interconnect
PXI	PCI eXtensions for Instrumentation

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter 2 a description of the i3002 hardware can be found. Chapter 3 covers the installation and setup of the card as well as mounting M-modules. In chapter 4 the operation and the usage of the i3002 is described. The i3002 is distributed with an APIS based demo application which is described in chapter 5. Finally this document contains an annex containing a bibliography, component image, technical data and the document history.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The i3002 provides a high-performance CompactPCI bus gateway to the M-module interface. The i3002 has a 3U form factor. Two M-modules can be mounted on the i3002.

The M-module interface of the i3002 complies with the M-module specification. The M-module specification is ANSI approved. The M-module interface features A8, A24, D16 and D32 access types.

The PCI interface is PCI Specification 2.2 Compliant, slave only. The PCI to M-module bridge is implemented using the PCI9030 PCI Bus Target Interface Chip of PLX Technology Inc.

2.2. TECHNICAL OVERVIEW

Below an overview of the functionality of the i3002 is listed.

CompactPCI interface:
- CompactPCI Specification 2.0 R3.0 Compliant
- PCI Specification 2.2 Compliant
- 5V or 3.3V signaling voltage (VIO) supported
- 5V only power supply
- 32-bit PCI data bus
- supports Big/Little Endian Byte Conversion

M-module interface:
- two M-module Interfaces (A08/A24, D16/D32, TRIGI, TRIGO)
- INTA software-end-of interrupt supported

PXI
- five trigger lines compliant with PXI Specification 2.1
- routing of PXI trigger lines to M-module interface TRIGA, TRIGB

I/O Connections:
- M-module I/O via connector on the front of the M-module
- via CompactPCI connector to the PCI bus

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

3. INSTALLATION AND SETUP

3.1. UNPACKING THE HARDWARE

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. MOUNTING AN M-MODULE

Two M-modules can be fitted on the i3002 carrier board. To plug in a module, position the 2-row 40 pole or 3-row 60-pole M-module interface connector of the module above one of the M-module interface connectors of the i3002. Then push the module until the 40 or 60-pole header connector is positioned and press the module with care in its place.

Note: With 2-row M-modules row C of the M-module interface connector is left unoccupied.

The module can be secured in its position using two or four screws (M3 * 5mm), refer to figure 1 for the positions of the mounting screws.

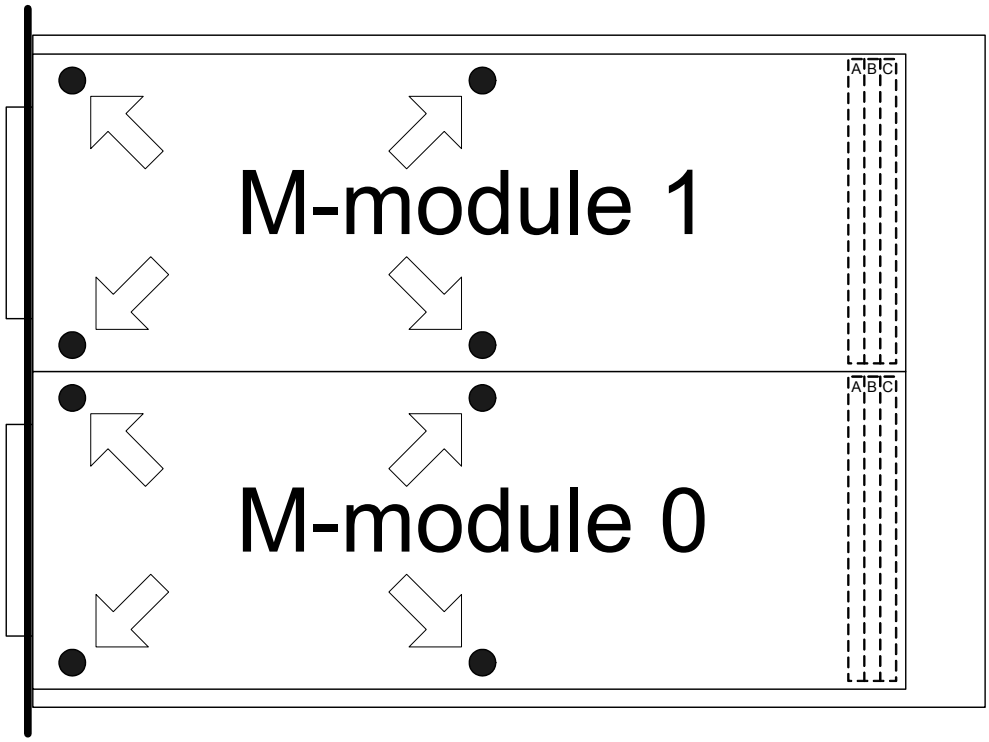

Figure 1 M-module mounting screws

3.3. GUIDE RAILS

To make it possible to use two M-modules in a 3U CompactPCI system, the i3002 carrier is slightly higher than a standard 3U card. To install the i3002 carrier in a standard CompactPCI system the special guide rails supplied with the card must be used.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

3.4. M-MODULE INTERFACE CONNECTOR

The interface between the i3002 carrier board and an M-module is realized with a 60 pole male header connector (rows A, B and C).

Pin Number	Row A	Row B	Row C
1	CS*	GND	AS*
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	DREQ*	D20
7	A06	DACK*	D21
8	A07	GND	D22
9	D08/A16	D00/A08	TRIGA
10	D09/A17	D01/A09	TRIGB
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	DS1*	DS0*	D29
18	DTACK*	WRITE*	D30
19	IACK*	IRQ*	D31
20	RESET*	SYSCLK	DS2*

Orientation of the 60 pole male header connector on the M-module:

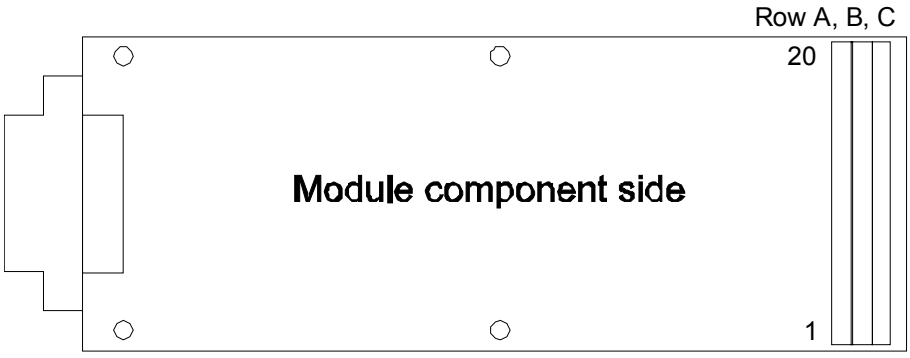

Figure 2 M-module Interface Connector

3.5. CompactPCI Interface Connector

The following table provides signal names for the CompactPCI J1 connector as used on the i3002.

Pin	A	B	C	D	E	F
1	+5 V	-12 V	TRST*	+12 V	+5 V	GND
2	TCK	+5 V	TMS	TDO	TDI	GND
3	INTA*	INTB*	INTC*	+5 V	INTD*	GND
4	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
5	BRSVP1A5	BRSVP1B5	RST*	GND	GNT*	GND
6	REQ*	GND	+3.3 V	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
9	C/BE[3]*	IDSEL	AD[23]	GND	AD[22]	GND
10	AD[21]	GND	+3.3 V	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]*	GND
12-14	Key area					
15	+3.3 V	FRAME*	IRDY*	GND	TRDY*	GND
16	DEVSEL*	GND	V(I/O)	STOP*	LOCK*	GND
17	+3.3 V	SDONE	SBO*	GND	PERR*	GND
18	SERR*	GND	+3.3 V	PAR	C/BE[1]*	GND
19	+3.3 V	AD[15]	AD[14]	GND	AD[13]	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
21	+3.3 V	AD[9]	AD[8]	M66EN	C/BE[0]*	GND
22	AD[7]	GND	+3.3 V	AD[6]	AD[5]	GND
23	+3.3 V	AD[4]	AD[3]	+5 V	AD[2]	GND
24	AD[1]	+5 V	V(I/O)	AD[0]	ACK64*	GND
25	+5 V	REQ64*	ENUM*	+3.3 V	+5 V	GND

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

The following tables lists the signals for the CompactPCI J2 connector as used on the i3002

Pin	A	B	C	D	E	F
1	-	-	-	-	-	GND
2	-	-	-	-	-	GND
3	-	-	-	-	-	GND
4	-	-	-	-	-	GND
5	-	-	-	-	-	GND
6	-	-	-	-	-	GND
7	-	-	-	-	-	GND
8	-	-	-	-	-	GND
9	-	-	-	-	-	GND
10	-	-	-	-	-	GND
11	-	-	-	-	-	GND
12	-	-	-	-	-	GND
13	-	-	-	-	-	GND
14	-	-	-	-	-	GND
15	-	-	-	-	-	GND
16	PXI_TRIG1	PXI_TRIG0	-	-	reserved	GND
17	PXI_TRIG2	-	-	-	-	GND
18	PXI_TRIG3	PXI_TRIG4	-	-	reserved	GND
19	-	-	-	-	-	GND
20	-	-	-	-	-	GND
21	-	-	-	-	-	GND
22	GA4	GA3	GA2	GA1	GA0	GND

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4. FUNCTIONAL DESCRIPTION

4.1. BLOCK DIAGRAM

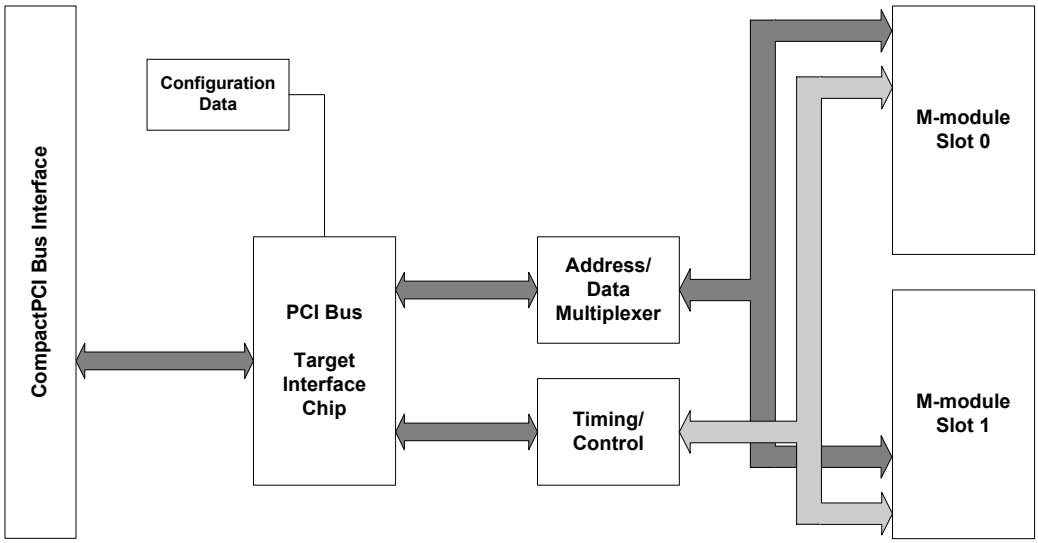

Figure 3 i3002 block diagram

4.2. PCI TO M-MODULE BRIDGE

The PCI to M-module bridge is implemented using the PCI9030 PCI Bus Target Interface Chip by PLX Technology Inc. in combination with an FPGA.

The PCI9030 supports both memory mapped and I/O mapped accesses from the PCI bus to the local M-module bus. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

The FPGA controls the timing of the M-module bus.

4.2.1. LOCAL BUS CONFIGURATION

The i3002 features a programmable local bus configuration which is used by both M-module slots. The local bus may be either 16 or 32 bit wide and may be multiplexed or non-multiplexed. The PCI9030 also offers big/ little endian byte swapping.

The PCI9030 offers four local address spaces which are not related to the two M-module slots. On the i3002 local address space 0 is configured for A8/D16 little endian memory mapped M-module and control register accesses and local address space 1 for A8/D16 little endian I/O mapped M-module and control register accesses and local address space 2 for A8/D32 little endian memory mapped M-module and control register accesses.

The following table gives an overview of the local address spaces.

Local Address Space	Access Type	Description
0	A08/D16	Memory mapped (little endian)
1	A08/D16	I/O mapped (little endian)
2	A08/D32	Memory mapped (little endian)

The local bus data lines LAD0 to LAD31 are connected to MD0 to MD31 M-module data lines. M-module accesses are asynchronous using the READY input of the PCI9030.

Configuration of the PCI interface and local address spaces is done through the PCI9030 configuration registers.

The table below gives an overview of the valid local addresses:

Local Address Range	Access Type	Description
0x0800 0000-0x0800 00FF	A08/D16	M-module 0
0x0800 0100		Interrupt control register 0
0x0800 0180-0x0800 01FF		Global Registers
0x0800 0200-0x0800 02FF	A08/D16	M-module 1
0x0800 0300		Interrupt control register 1
0x0800 0380-0x0800 03FF		Global Registers
0x0800 0800-0x0800 08FF	A08/D32	M-module 0
0x0800 0900		Interrupt control register 0
0x0800 0880-0x0800 08FF		Global Registers
0x0800 0A00-0x0800 0AFF	A08/D32	M-module 1
0x0800 0B00		Interrupt control register 1
0x0800 0B80-0x0800 0BFF		Global Registers
0x0000 0000-0x00FF FFFF	A24/D16	M-module 0
0x0100 0000-0x01FF FFFF	A24/D16	M-module 1
0x0400 0000-0x04FF FFFF	A24/D32	M-module 0
0x0000 0000-0x00FF FFFF	A24/D32	M-module 1

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4.2.2. INTERRUPTS

On the i3002 there are three types of interrupts, M-module interrupts, timeout interrupts and address error interrupts. M-module interrupts are connected to LINT1 of the PCI9030, timeout interrupts and address error interrupts are connected to LINT2 of the PCI9030.

Each M-module slot has its own interrupt control register to enable and check the status of the M-module interrupt. Refer to section 4.4.1 for more information about the interrupt control register. For information on programming and configuration of the PCI9030 please refer to the PCI9030 data sheet.

4.2.3. CONFIGURATION EEPROM

After reset the PCI9030 reads a serial EEPROM on the card containing factory settings. Default local address space 0 of the PCI9030 is configured for A08D16 type of M-module accesses mapped in memory space and local address space 1 is configured for A08D16 type of M-module accesses mapped in I/O space.

The table below shows the contents of the serial EEPROM on a standard i3002.

Offset	Content	Register	Description
00	3090	Device ID	PCIIDR[31:16]
02	10B5	Vendor ID	PCIIDR[15:0]
04	0280	PCI Status	PCISR[15:0]
06	0000	PCI Command	Reserved
08	0801	Class Code	PCICCR[15:0]
0A	0001	Class Code / Revision	PCICCR[7:0]/PCIREV[7:0]
0C	3002	Subsystem ID	PCISID[15:0]
0E	10B5	Subsystem Vendor ID	PCISVID[15:0]
10	0000	MSB New Capability Pointer	Reserved
12	0040	LSB New Capability Pointer	CAP_PTR[7:0]
14	0000	(Maximum latency and Minimum Grant are not loadable)	Reserved
16	0100	interrupt Pin (Interrupt Line Routing is not loadable)	PCIIPR[7:0]/PCIILR[7:0]
18	4801	MSW of Power Management Capabilities	PMC[15:11,5,3:0]
1A	0001	LSW of Power Management Next Capability Pointer/Power Management Capability ID	PMNEXT[7:0] / PMCAPID[7:0]
1C	0000	MSW of Power Management Data/PMCSR Bridge Support Extension	Reserved
1E	0000	LSW of Power Management Control/Status	PMCSR[14:8]
20	0000	MSW of Hot Swap Control/Status	Reserved
22	0000	LSW of Hot Swap Next Capability Pointer/Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]
24	0000	PCI Vital Product Data Address	Reserved

Offset	Content	Register	Description
26	0003	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[7:0] / PVPDCNTL[7:0]
28	0FFF	MSW of Local Address Space 0 Range	LAS0RR[31:16]
2A	FC00	LSW of Local Address Space 0 Range	LAS0RR[15:0]
2C	0FFF	MSW of Local Address Space 1 Range	LAS1RR[31:16]
2E	FF01	LSW of Local Address Space 1 Range	LAS1RR[15:0]
30	0000	MSW of Local Address Space 2 Range	LAS2RR[31:16]
32	0000	LSW of Local Address Space 2 Range	LAS2RR[15:0]
34	0000	MSW of Local Address Space 3 Range	LAS3RR[31:16]
36	0000	LSW of Local Address Space 3 Range	LAS3RR[15:0]
38	0000	MSW of Expansion ROM Range	EROMRR[31:16]
3A	0000	LSW of Expansion ROM Range	EROMRR[15:0]
3C	0200	MSW of Address Space 0 Local Base Address (Remap)	LAS0BA[31:16]
3E	0001	LSW of Address Space 0 Local Base Address (Remap)	LAS0BA[15:0]
40	0200	MSW of Local Address Space 1 Local Base Address (Remap	LAS1BA[31:16]
42	0001	LSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[15:0]
44	0000	MSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[31:16]
46	0000	LSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[15:0]
48	0000	MSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[31:16]
4A	0000	LSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[15:0]
4C	0000	MSW of Expansion ROM Local Base Address (Remap)	EROMBA[31:16]
4E	0000	LSW of Expansion ROM Local Base Address (Remap)	EROMBA[15:0]
50	0040	MSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[31:16]
52	0002	LSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[15:0]
54	0040	MSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[31:16]
56	0002	LSW of Local Address Space 1 bus Region Descriptor	LAS1BRD[15:0]

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

Offset	Content	Register	Description
58	0000	MSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[31:16]
5A	0000	LSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[15:0]
5C	0000	MSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[31:16]
5E	0000	LSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[15:0]
60	0000	MSW of Expansion ROM Bus Region Descriptor	EROMBRD[31:16]
62	0000	LSW of Expansion ROM Bus Region Descriptor	EROMBRD[15:0]
64	0200	MSW of Chip Select 0 Base Address	CS0BASE[31:16]
66	0281	LSW of Chip Select 0 Base Address	CS0BASE[15:0]
68	0000	MSW of Chip Select 1 Base Address	CS1BASE[31:16]
6A	0000	LSW of Chip Select 1 Base Address	CS1BASE[15:0]
6C	0000	MSW of Chip Select 2 Base Address	CS2BASE[31:16]
6E	0000	LSW of Chip Select 2 Base Address	CS2BASE[15:0]
70	0000	MSW of Chip Select 3 Base Address	CS3BASE[31:16]
72	0000	LSW of Chip Select 3 Base Address	CS3BASE[15:0]
74	0030	Serial EEPROM Write-Protected Address Boundary	PROT_AREA[7:0]
76	0000	LSW of Interrupt Control/Status	INTCSR[15:0]
78	0078	MSW of PCI Target Response, Serial EEPROM, And Initialization Control	CNTRL[31:16]
7A	4000	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[15:0]
7C	0024	MSW of General Purpose I/O Control	GPIOC[31:16]
7E	9000	LSW of General Purpose I/O Control	GPIOC[15:0]

Warning: Reprogramming of the serial EEPROM is strongly discouraged because improper EEPROM contents may cause system boot problems which may require EEPROM replacement.

4.3. M-MODULE INTERFACE

The i3002 provides an M-module interface to a CompactPCI based platform. The wide range of standardized M-modules includes not only process I/O modules but also interface extensions, field buses, DSP and motion control modules as well as special-purpose functions.

The i3002 has the following M-module features:
- 3 -row M-modules supported
- 2-row M-modules supported
- A08/A24, D16/D32 address/data range
- INTA supported
- TRIGI, TRIGO supported

4.3.1. STANDARD ACCESSES

The standard M-module interface has an 8-bit address bus. Timing during access is determined solely by the signal SELECT* and DTACK*. This substantially decreases the circuit complexity on the M-modules. On M-modules supporting extended address space, the standard M-module access can be used as an I/O cycle to distinguish between memory type access and register type access.

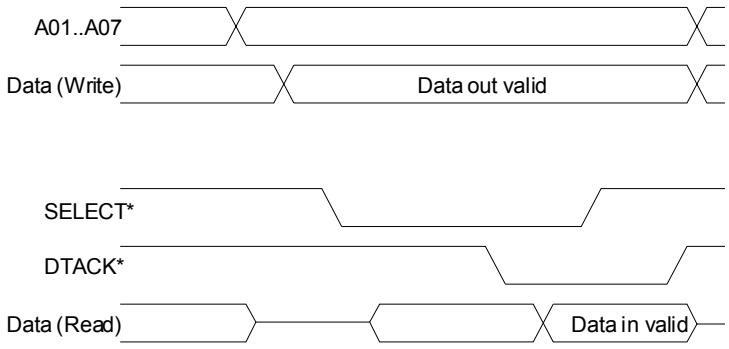

Figure 4 Standard read/write transfer

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4.3.2. EXTENDED ACCESSES

The extended address space enables M-modules to be used for applications extending beyond typical I/O functions. The i3002 supports M-modules up to a 24-bit address bus. The address information is transferred across the data bus in multiplexed mode, reducing the number of pins required. An additional line AS* indicates the current use of the bus. The standard M-module store cycle is embedded in the address transfer cycle.

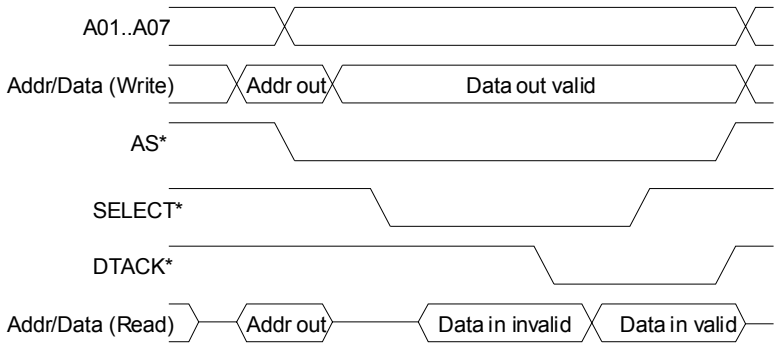

Figure 5 Extended read/write transfers

By mapping both standard and extended M-module access in a different address space as seen from the carrier board, a distinction between a standard and extended M-module access can be made. The table below gives an overview of the local address map in relation to the M-module access type.

Local Address	M-module Access Type
0x08000000	A08/D16
0x08000800	A08/D32
0x00000000	A24/D16
0x04000000	A24/D32

Note: Since the standard M-module access is embedded into the extended M-module access, it is also possible to access a standard M-module in the A24 address range, however since the addresses must be multiplexed, this will result in a slightly slower access.

4.3.3. BUS TIMER

If an M-module transfer timeout occurs, the i3002 will generate a DTACK*, to prevent the system from lock-out.

The transfer timeout is defined as the SELECT* to DTACK* time which is 10 useconds, conforming the M-module Specification.

An interrupt is generated when a transfer timeout occurs, this interrupt is connected to LINT2 of the PCI9030. See “Interrupt Status Control Register” on page 23.

4.3.4. TRIGGER LOGIC

The i3002 provides very flexible trigger capabilities. Each of the PXI trigger lines (PXI_TRIG[4..0]) can be used as a source or a destination for the M-module interface trigger signals TRIGA and TRIGB.

In addition the i3002 provides two independently programmable trigger generators which are driven by a common prescaler clock. The output of these trigger frequencies FREQA and FREQB can be set between 8MHz and 243.2Hz. See Figure 6 for a block diagram of the trigger generators

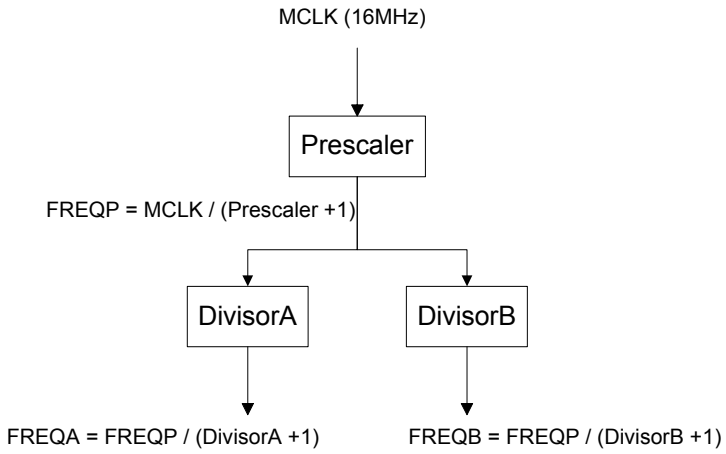

Figure 6 Trigger Generators

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4.4. CONTROL REGISTERS

	Offset from M-module base	Description
Specific	0x100	Interrupt Status and Control
Global (common to all M-modules)	0x180	Trigger A Divisor
	0x184	Trigger B Divisor
	0x188	Trigger A Control
	0x18C	Trigger B Control
	0x190	Trigger Prescaler
	0x194	Geographic Address

4.4.1. INTERRUPT STATUS CONTROL REGISTER

With the interrupt status control register the interrupts of the i3002 can be controlled. Each M-module slot has its own interrupt status control register and is located at offset 0x100 relative to the local address of the M-module.

IC_REG Offset: 0x100

15 ... 4	3	2	1	0
not used	AE	TO	IE	IA
Reset:				
	0	0	0	0
Read / Write				

IA Interrupt Active
This status bit is asserted when there is an interrupt request from the M-module. The M-module interrupt is connected to LINT1 of the PCI9030.

IE Interrupt Enable
Set this bit to enable M-module interrupts. Clear this bit to disable M-module interrupts.

TO Timeout
When asserted, a transfer timeout has occurred and a timeout interrupt has been generated. Clear pending interrupt by writing a ‘0' to it. The timeout interrupt is connected to LINT2 of the PCI9030.

AE Address Error
When asserted, the PCI bus master has requested single bytes in different words of a double word. This error only occurs in D32 mode and generates an address error interrupt which is connected to LINT2 of the PCI9030. Clear error by writing a ‘0’ to it.

Note: Interrupts must also be enabled on the PCI9030. Refer to PCI9030 data sheet for more information about enabling interrupts.

4.4.2. TRIGGER CONTROL REGISTERS

The following registers will describe the trigger registers. There is one global set of trigger registers available on the i3002. These global registers are mirrored within each M-module slot address space.

TRIGADIV Offset: 0x180

15 … 8	7 … 0
not used	DivisorA
Reset:	
	0
Read / Write	

DivisorA[7..0]
This byte provides the divisor for further dividing the clock derived from the prescaler. If enabled in the Trigger Control register (TRIGACTRL) the resulting clock (FREQA) is output on TRIGA. FREQA can be calculated using the following formula:

$$FREQA = \frac{FREQP}{DivisorA}$$

TRIGBDIV Offset: 0x184

15 … 8	7 … 0
not used	DivisorB
Reset:	
	0
Read / Write	

DivisorB[7..0]
This byte provides the divisor for further dividing the clock derived from the prescaler. If enabled in the Trigger Control register (TRIGBCTRL) the resulting clock (FREQB) is output on TRIGB. FREQB can be calculated using the following formula:

$$FREQB = \frac{FREQP}{DivisorB}$$

TRIGACTRL Offset: 0x188

15 … 8	7 … 5	4 … 2	1	0
not used	FAR	TAR	TAD	TAEN
Reset:				
	0	0	0	0
Read / Write				

FAR[7..5]Frequency A Route
These bits determine on which of the PXI_TRIG[4..0] trigger lines FREQA will be routed:

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

FAR[7..5]	Description
0 0 0	Not Routed
0 0 1	PXI_TRIG4
0 1 0	PXI_TRIG3
0 1 1	PXI_TRIG2
1 0 0	PXI_TRIG1
1 0 1	PXI_TRIG0
others	reserved

TAR Trigger A Route
These bit determine which trigger source is routed to TRIGA (if TRIGA is configured as an output, TAD is set to ‘0’) or to which destination TRIGA is routed (if TRIGA is configured as an input, TAD is set to ‘1’)

TAR[4..2]	TRIGA output (TAD is ‘0’)	TRIGA input (TAD is ‘1’)
0 0 0	FREQA (internally generated)	reserved
0 0 1	PXI_TRIG4	PXI_TRIG4
0 1 0	PXI_TRIG3	PXI_TRIG3
0 1 1	PXI_TRIG2	PXI_TRIG2
1 0 0	PXI_TRIG1	PXI_TRIG1
1 0 1	PXI_TRIG0	PXI_TRIG0
others	reserved	reserved

TAD Trigger A Direction
This bit determines the direction of the TRIGA line on the M-module interface. If this bit is set to ‘0’, TRIGA is used as an output which means the signal is driven to the M-module, if TAD is set to ‘1’, TRIGA is used as an input which means the signal is received from the M-module.

TAEN Trigger A Enable
This bit is used (if TRIGA is configured as an output, TAD is set to ‘0’) to enable the TRIGA output signal. If this bit is set to ‘0’, the TRIGA output is disabled. If this bit is set to ‘1’, the TRIGA output is enabled.

TRIGBCTRL Offset: 0x18C

15 … 8	7 … 5	4 … 2	1	0
not used	FBR	TBR	TBD	TBEN
	0	0	0	0

Reset:

Read / Write

FBR[7..5]Frequency B Route
These bits determine on which of the PXI_TRIG[4..0] trigger lines FREQB will be routed:

FBR[7..5]	Description
0 0 0	Not Routed
0 0 1	PXI_TRIG4
0 1 0	PXI_TRIG3
0 1 1	PXI_TRIG2
1 0 0	PXI_TRIG1
1 0 1	PXI_TRIG0
others	reserved

TBR Trigger B Route
These bit determine which trigger source is routed to TRIGB (if TRIGB is configured as an output, TBD is set to '0') or to which destination TRIGB is routed (if TRIGB is configured as an input, TBD is set to '1')

TBR[4..2]	TRIGB output (TBD is '0')	TRIGB input (TBD is '1')
0 0 0	FREQB (internally generated)	reserved
0 0 1	PXI_TRIG4	PXI_TRIG4
0 1 0	PXI_TRIG3	PXI_TRIG3
0 1 1	PXI_TRIG2	PXI_TRIG2
1 0 0	PXI_TRIG1	PXI_TRIG1
1 0 1	PXI_TRIG0	PXI_TRIG0
others	reserved	reserved

TBD Trigger B Direction
This bit determines the direction of the TRIGB line on the M-module interface. If this bit is set to '0', TRIGB is used as an output which means the signal is driven to the M-module, if TBD is set to '1', TRIGB is used as an input which means the signal is received from the M-module.

TBEN Trigger B Enable
This bit is used (if TRIGB is configured as an output, TBD is set to '0') to enable the TRIGB output signal. If this bit is set to '0', the TRIGB output is disabled. If this bit is set to '1', the TRIGB output is enabled.

TRIGPRESC Offset: 0x190

15 … 8	7 … 0
not used	Prescaler
Reset:	
	0
Read / Write	

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

Prescaler[7..0]

This byte provides the divisor for dividing the local bus clock (16MHz). The resulting clock is used to generate the internally generated clocks for TRIGA (FREQA) and TRIGB (FREQB). If the prescaler is set to 0x00 the internally generated clock is disabled. FREQP can be calculated using the following formula:

$$FREQP = \frac{MCLK}{(Prescaler + 1)}$$

4.4.3. GEOGRAPHIC ADDRESS REGISTER

This global register is mirrored within each M-module slot address space.

GAR Offset: 0x194

15 … 8	7 … 5	4 … 0
not used	RES	GA
	0	

Reset:

Read Only

RES[7..5]

These reserved bits are hardwired to zero

GA[4..0]Geographic Address

These bits are the geographic address bits as defined by the CompactPCI specification to provide easy identification of the physical slot in which the i3002 is inserted.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

5. SOFTWARE SUPPORT

The i3002 comes with an APIS based application that scans the PCI bus for M-modules, modscan. For interfacing the PXI trigger logic a software library is available. This chapter gives a short description of APIS, the usage of the modscan application and the PXI trigger logic library.

5.1. APIS

AcQ produces and markets a large number of standard M-modules varying from networking and process I/O to motion control applications. Physically, the M-modules are supported by a large number of hardware platforms: VMEbus, PCI, CompactPCI as well as a wide variety of operating systems: OS-9, Windows NT, Linux etc.

APIS (AcQ's Platform Interface Software) offers a way to program platform independent applications, example- and test software for controlling hardware. Application software written for APIS must only need re-compiling for a particular platform and must be operational with little effort (provided that the application is operating system independent). APIS support for i3002 is currently available for DOS, Windows 95/98/2000/ NT/XP, Linux and Solaris. Please check our website for up-to-date APIS support information. Refer to the APIS Programmer's Manual for more information about APIS.

5.2. MODSCAN

Modscan is an APIS based application that scans the PCI bus for M-modules. The program can be called from the command line and detects all AcQuisition Technology's PCI based M-module carrier boards (i2000, i3000, i3100 etc.). The IDs of the M-modules present on the carrier are displayed. When an M-module does not have an identification EEPROM, ‘Unknown M-module' is displayed. If a slot on a carrier is not occupied with an M-module, it is not displayed in the output.

The display output of modscan may look as follows:

```
M-module scan software by
AcQuisition Technology B.V. 2002

Slot 0: M321
Slot 1: M302
Slot 3: Unknown M-module
Slot 4: M395

Program closed
```

5.3. PXI TRIGGER LOGIC LIBRARY

The PXI trigger logic library is actually an ANSI-C source code file containing register definitions and APIS based function macros providing user friendly access to the i3002’s PXI trigger logic. The library is distributed as a zip archive with the following contents:

/PROJECT/PXITRIG/SOFTWARE/LIB/i3002pxi.h

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

6. ANNEX

6.1. BIBLIOGRAPHY

M-Module Standard: ANSI/VITA 12-1996, M-Module Specification;
VITA, PO Box 19658, Fountain Hills, AZ 85269, USA
Phone (1)(480)8377486
http://www.vita.com

PCI9030 PCI Bus Target Interface Chip Data sheet
PLX Technology INC, 390 Potrero Ave, Sunnyvale, CA 94086, USA.

PCI Local Bus Specification Revision 2.2
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI BIOS Specification Revision 2.1
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344
http://www.pcisig.com

PCI System Architecture, Third Edition
Tom Shanley/Don Anderson
ISBN: 0-201-40993-3

CompactPCI Specification 2.0 Revision 3.0
PCI Industrial Computer Manufacturers Group, 401 Edgewater Place, Wakefield, MA01880, USA
Phone (1)(781)2469318, Fax (1)(781)2241239
http://www.picmg.com

PXI Hardware Specification Revision 2.1
PXI Systems Alliance.
http://www.pxisa.org

6.2. COMPONENT IMAGE

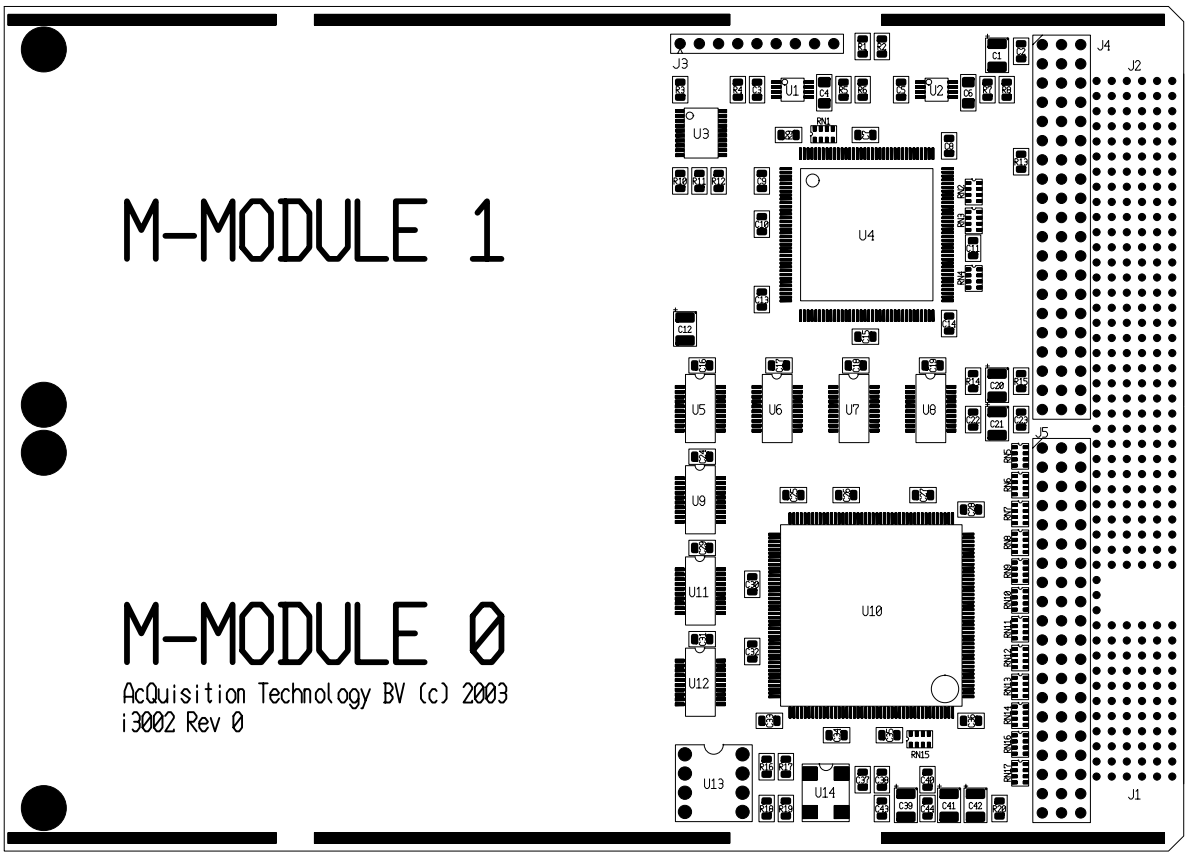

Figure 7 i3002 Component image

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

6.3. TECHNICAL DATA

Slots on the base-board:
Requires one CompactPCI slot.

Connection:
To base-board via CompactPCI connector.
2x M-module interface.

Power supply:
+5VDC ±10%, typical 400mA (without an M-module mounted)

Temperature range:
Operating: 0..+60 C.
Storage: -20..+70 C.

Humidity:
Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release