U S E R ' S M A N U A L

VXI
96 CHANNEL
STATIC
DIGITAL
MODULE

MODEL
VX442C

Manual Part No: 11028634A

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INTRODUCTION

This manual describes the operation and maintenance requirements of the C&H model VX442C 96 Channel Static Digital VXI module. These modules represent a subset of the test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual is information on the physical and electrical specifications, installation and startup procedures, operating procedures, functional description, figures and diagrams required to adequately use this product.

The part numbers covered by this manual are:

Part Number	Description
11028630-0001	96 Channel Static Digital Module

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1.0 GENERAL DESCRIPTION

The 96 channel static digital module is a VXIbus compatible device that provide general purpose digital drive/receive capability. The module features drive/sense/mask capabilities along with interrupt and trigger functions.

1.1 PURPOSE OF EQUIPMENT

This module is well suited for applications within ATE systems, data acquisition systems, communications interface, hardware-in-the-loop simulation systems as well as development laboratory environments.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- 96 Digital Input/Output Pins
- Versatile triggering allows synchronization of multiple boards
- Immediate and Delayed Trigger (Data Latch) Capability
- VXI Interrupt Support
- Full drive/sense/mask with interrupt on failure
- Read back capability of all driver states
- Output drive enable/disable
- Socket mounted drive and sense devices

1.2.2 Electrical

The module only requires the +5V supply from the VXI backplane. The peak module current (I_{PM}) is 1.8 amps.

The actual power requirements will depend on the driver characteristics and output loading. Below are the input and output characteristics for the various configurations:

OUTPUT CHARACTERISTICS:

Device Type:	74ABT126
V_{OH}	3.0 V min.
V_{OL}	0.35 V max.
I_{OH}	-32 mA max.
I_{OL}	64 mA max.

INPUT CHARACTERISTICS: (see notes 1 and 2)

Device Type:	74ALS245
V_{IH}	2.0 V min
V_{IL}	0.7 V max
I_{IH}	20.0 µA max
I_{IL}	-0.1 mA max

NOTES:

1) The inputs have 100KΩ pull-up resistors, which have a minor (50µA) effect on the input characteristics.
2) The pull-up resistors on the inputs provide a stable high level for unconnected channels.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the VXIbus specification Rev 1.4 for single slot size 'C' modules. The nominal dimensions are 233.35 (9.187 in) high x 340 mm (13.386 in) deep.

1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +55°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

1.2.5 Bus Compliance

The module complies with the VXIbus Specification Revision 1.4 for C-size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821 and IEC 822.

Module:	C-size, single slot	Data Transfer:	D16 Slave
Device Type:	Register Based	Memory Space:	None
Manufacturer ID:	$FC1_{16}$	Interrupts:	None
Model Code:	$FFF1_{16}$	TTL Triggers	Supported
Addressing:	A16	Bus Arbitration:	BRx tied to BGx

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the VX442C is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and plastic bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The VX442C contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION

> CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

Set or verify the module's logical address. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 4.0 (Operating Instructions).

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof plastic bag. Heat seal or tape the plastic bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The VXI-compatible VX442C is configured, controlled, and statused through on-board registers accessible through the VXI backplane. The drive devices provide significant drive current capability and both the drive and sense devices are socket mounted for ease of maintenance.

The digital output level of each pin is controlled by writing to an 8-bit output register. The input values can be read on-the-fly or configured to latch their value on software command, on receipt of an external trigger, or on a comparison error following a trigger. Data can be latched immediately on receipt of a trigger or be latched after a programmed delay following a trigger. A trigger signal can also be generated on one of the P2 TTLTRG* lines. This versatile trigger and data hold capability allows a system of multiple cards to latch data synchronously across the backplane. Interrupts can be generated on the occurrence of a trigger or on a comparison error.

A functional block diagram of the module is shown in Figure 1.

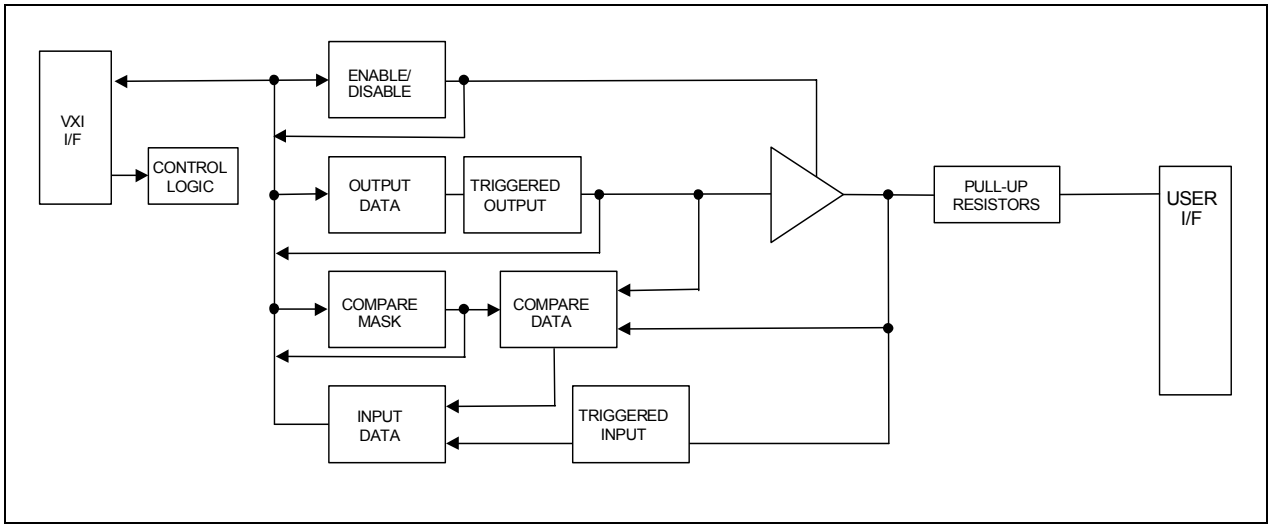


Figure 1. Functional Block Diagram

3.2 SWITCH CONFIGURATON

Before placing the module in a chassis, the logical address and the trigger count reference clock count switches must be selected. The switches are accessible though the sides vents of the top shield. The shield does not have to removed to set the switches. The locations of each of these options is shown in Figure 2.

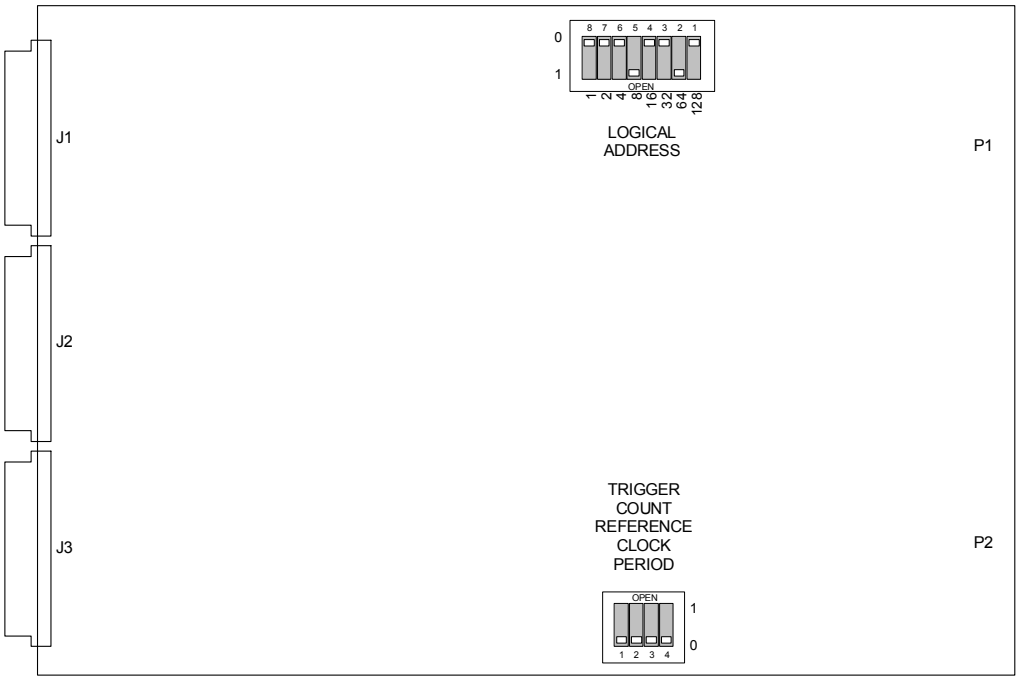


Figure 2. Hardware Configurable Controls

3.2.1 Logical Address Selection

An 8-bit logical address switch is provided to uniquely identify the module in the system. The switch location is shown in Figure 2.

3.2.2 Trigger Count Reference Clock Period Selection

These switches are used to select the clock period for trigger (delay) count reference clock. See section 3.6.1 for details. The location of the swithces is shown in Figure 2.

3.2.3 Input/Output Termination

The VX442C has provisions for customizing the input/output termination. The standard unit comes with 100KΩ pull-up resistors and 0Ω series output resistors, however, customized input/output termination is easily accomadated. Contact C&H for more information.

3.3 INDICATORS

Two LED indicators are provided on the front panel. One indicates modules access and the other identifies the module in the chassis.

ACCESS: This front panel LED illuminates whenever the module is properly accessed by the host processor.

MODID: This front panel LED illuminates whenever the host processor applies the MODID signal to the slot the module is occupying.

3.4 CONNECTORS

3.4.1 Front Panel Connectors

The I/O interface is through three 78 pin receptacle, metal shell, HD-22 (w/screwlocks) style connectors (AMP P/N 748483-6) located on the front panel of the module. Each connector contains 32 I/Os and a trigger input signal for four ports. A ground pin is provide for each I/O and trigger signal. Each of the three connectors have similar pin definitions to allow attaching cables to be the same. See Figure 3 for connector locations and Appendix B for complete pin definitions.

3.4.2 Rear Connectors

3.4.2.1 P1 Connector

The P1 connector is configured in accordance with the VXI P1 specification. (See Appendix B)

3.4.2.2 P2 Connector

The P2 connector is configured in accordance with the VXI P2 specification with utilization of the TTL Trigger lines (TTLTRGx*) (See Appendix B).

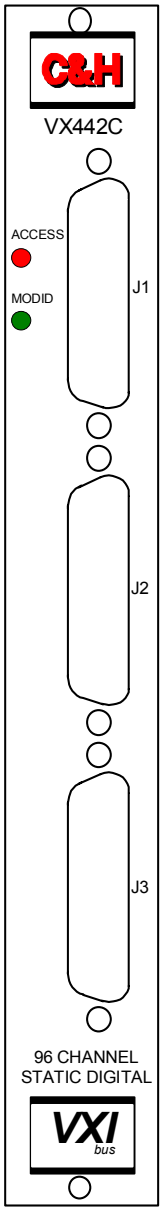


Figure 3. Front Panel

3.5 CONFIGURATION REGISTERS

There are several types of registers used to configure and control the VX442C. The VXI configuration registers provide for control and status as required by the VXIbus specification. The General Status/Control register provides board-level control and status. The Port Registers provide port level control and status. An address map of the registers is shown in Table I.

Table I. VXI Register Address Map

Addr (Hex)	Write Register Description		Read Register Description	
Base + 16	Write Port 10	Write Port 11	Read Port 10	Read Port 11
Base + 14	Write Port 8	Write Port 9	Read Port 8	Read Port 9
Base + 12	Write Port 6	Write Port 7	Read Port 6	Read Port 7
Base + 10	Write Port 4	Write Port 5	Read Port 4	Read Port 5
Base + 0E	Write Port 2	Write Port 3	Read Port 2	Read Port 3
Base + 0C	Write Port 0	Write Port 1	Read Port 0	Read Port 1
Base + 0A	Interrupt Control Register		Interrupt Status Register	
Base + 08	General Control Register		General Status Register	
Base + 06	VXI Unused Register		VXI Unused Register	
Base + 04	VXI Control Register		VXI Status Register	
Base + 02	VXI Read Only Register		VXI Device Type Register	
Base + 00	VXI Read Only Register		VXI ID Register	
Bit	15 08	07 00	D15 . . . . .D08	D07 . . . . D00

3.5.1 VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in Figure 4.

VXI Identification (ID) Register (Base + 00h) - A read of this register provides manufacturer identification, device classification (i.e., register based), and the addressing mode (A16). A write to this register has no effect.

VXI Device Type Register (Base + 02h) - A read of this register provides the model code identifier. A write to this register has no effect.

VXI Status/Control Register (Base + 04h) - A read of this register provides the state of P2 MODID* line, and the Ready and self-test Passed status. A write to bit 0 of this register provides a reset of the module. SYSFAIL* is not implemented on this module.

00	VXI ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Not Used							
Read	Device Class		Address Space		Manufacturer ID											

Device Class ⇒ Device Class (Register Based = binary 11)
Address Space ⇒ Address Space (A16 Only = binary 11)
Manuf. ID ⇒ Manufacturer Identification (C & H Technologies = hex FC1)

02	VXI DEVICE TYPE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used															
Read	Model Code															

Model Code ⇒ Model code (C&H Model VX442C = hex FFF1)

04	VXI Status/Control															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used															Rst
Read	0	MOD ID*	1	1	1	1	1	1	0	0	0	0	Rdy	Pass	1	1

Rst ⇒ Reset
MOD ID* ⇒ Module ID Status (0 = P2 MODID* line is selected (active-high))
Rdy ⇒ Ready
Pass ⇒ Self-test pass/fail indicator

Figure 4. VXI Configuration Registers

3.5.2 General Status/Control Register

This register provides control and status of the board-level trigger and comparison options and is used to select the function of the Port Register. Details are shown in Figure 5.

08	GENERAL STATUS/CONTROL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SBT	TE	-	-	TS	Trig Sel			Trig Count				-	Port Function		
Read	SBT	TE	-	CMP	TS	Trig Sel			Trig Count				-	Port Function		

SBT ⇒ Software Board Trigger (1 = Generate an internal board trigger)
TE ⇒ Output Trigger Enable (1 = Enable, 0 = Disable)
CMP ⇒ Compare Status (0 = Error occurred, 1 = No error)
TS ⇒ Trigger Source (0 = Board Trigger, 1 = TTLTRGx*)
Trig Sel ⇒ TTLTRGx* Select

bit 10	9	8	
0	0	0	TTLTRG0*
0	0	1	TTLTRG1*
	⋮		
1	1	1	TTLTRG7*

Trig Count ⇒ Trigger Delay Count (Delay = Count Ref. Clk Period × Trig Count) (see notes)
Port Function ⇒ Port Register Function Select

bit 2	1	0	
0	0	0	Read Data / Write Data
0	0	1	Read Feedback / Write Data
0	1	0	Read Enable / Write Enable
0	1	1	Read Mask / Write Mask
1	0	0	Read Status / Write Control
1	0	1	Not Used
1	1	X	Not Used

Notes:
1. Trig Count must be greater than zero to use any internal trigger.
2. Trigger delay uses an asynchronous clock and, therefore, may be up to one Count Ref. Clock Period short depending on the timing of the trigger signal with respect to the clock edge.

Figure 5. General Status/Control Register

0A	INTERRUPT CONTROL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-			-	-	IRQ Sel			IRQ Vector/L. A.							
Read	-			IP*	-	IRQ Sel			IRQ Vector/L. A.							

IP* ⇒ Interrupt Pending (0 = Interrupt Pending, Read Only)

IRQ Sel ⇒ Interrupt Channel Select

bit 10	9	8	
0	0	0	Interrupt Disabled
0	0	1	IRQ1*
.	.	.	
.	.	.	
1	1	1	IRQ7*

IRQ Vector/L.A. ⇒ Interrupt Vector / Logical Address (For VXI compliant interrupts, set these bits equal to the Logical Address assigned to the card)

Figure 6. Interrupt Control Register

3.5.3 Port Registers

The ports are controlled and monitored through multiple 8-bit registers. The General Control register (Base + 08h) is used to select the desired function register as shown in Figure 5. The following function registers are used to control the input, output and function of the port as detailed in Figure 7.

Port Data Register (000) On write, this register controls the data pattern output to the front panel connectors. This pattern is also used as the unmasked expected value in the compare operation. On read, this register presents either the input data pattern present at the front panel input connectors or the bits failing the comparison operation. If the Read Mode in the Port Status/Control Register is set to a 0, then the input data pattern is read. If set to a 1, the comparison result is read. Positive logic is used.

Output Read Back Register (001) On write, this register performs the same function as writing to the Port Data Register (i.e., it controls the output data pattern). On read, it provides "read back" of the latched output data for write verification and diagnostics. Note that the data read back is dependent on the trigger mode, since the data read back is the Triggered Output data as shown in Figure 1.

Port Enable/Disable Register (010) This read/write register enables or disables the output drivers. A low (0) disables the output of the respective driver, a high (1) enables the output driver.

Mask Register (011) This read/write register is used to mask compare errors between the received value and the expected value. The received value is the input data pattern and the expected value is the last pattern written to the Port (Output) Data Register. Any bits in error are logically ANDed with the 1's complement of the mask pattern.

Port Status/Control Register (100) This read/write register controls and provides status of various trigger, latching, and read modes.

Func: 000	PORT DATA REGISTER															
	PORTS 0, 2, 4, 6, 8 & 10								PORTS 1, 3, 5, 7, 9 & 11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Output/Expected Data Pattern								Output/Expected Data Pattern							
Read	Input/Failed Bits Data Pattern								Input/Failed Bits Data Pattern							

On write - Data written is output to driver and is used as expected value for compare operation
On read - If Read Mode = 0 then input data pattern is read,
If Read Mode = 1 then bits failing comparison are read as 1's

Func: 001	PORT OUTPUT READBACK REGISTER															
	PORTS 0, 2, 4, 6, 8 & 10								PORTS 1, 3, 5, 7, 9 & 11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Output/Expected Data Pattern								Output/Expected Data Pattern							
Read	Latched Output Pattern								Latched Output Pattern							

Func: 010	PORT ENABLE/DISABLE REGISTER															
	PORTS 0, 2, 4, 6, 8 & 10								PORTS 1, 3, 5, 7, 9 & 11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Enable/Disable Output Driver Pattern								Enable/Disable Output Driver Pattern							
Read	Enable/Disable Pattern								Enable/Disable Pattern							

Func: 011	PORT MASK REGISTER															
	PORTS 0, 2, 4, 6, 8 & 10								PORTS 1, 3, 5, 7, 9 & 11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Compare Mask Pattern								Compare Mask Pattern							
Read	Compare Mask Pattern								Compare Mask Pattern							

Figure 7. Port Registers (1 of 2)

Func: 100	PORT STATUS/CONTROL REGISTER															
	PORTS 0, 2, 4, 6, 8 & 10								PORTS 1, 3, 5, 7, 9 & 11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	TRIG FUNC				SPT	RM	HMODE		TRIG FUNC				SPT	RM	HMODE	
Read	TRIG FUNC				HS	RM	HMODE		TRIG FUNC				HS	RM	HMODE	

TRIG FUNC ⇒ Trigger Function* (see below)

bit 15/7	14/6	13/5	12/4	INPUT DATA	OUTPUT DATA
0	0	0	X	Immediate Read	Immediate Output
0	0	1	0	Latch on immediate trig in	Immediate Output
0	0	1	1	Latch on delayed trig in	Immediate Output
0	1	X	0	Latch on rising edge of port trigger	Immediate Output
0	1	X	1	Latch on falling edge of port trigger	Immediate Output
1	0	0	0	Immediate Read	Output data on immediate trig in
1	0	0	1	Immediate Read	Output data on delayed trig in
1	0	1	0	Latch on immediate trig in	Output data on immediate trig in
1	0	1	1	Latch on delayed trig in	Output data on immediate trig in
1	1	0	0	Latch on rising edge of port trigger	Output data on rising edge of port trigger
1	1	0	1	Latch on falling edge of port trigger	Output data on rising edge of port trigger
1	1	1	0	Latch on rising edge of port trigger	Output data on falling edge of port trigger
1	1	1	1	Latch on falling edge of port trigger	Output data on falling edge of port trigger

SPT ⇒ Software Port Trigger (a 1 generates a TTLTRGx* pulse (~100 ns))

HS ⇒ Hold Status (1 = data is being held)

RM ⇒ Read Mode (0 = input data, 1 = fail bits)

HMODE ⇒ Hold Mode

bit 9/1	8/0	
0	0	Hold disabled / reset
0	1	Hold on compare error after trigger
1	X	Hold on trigger

*Note: An immediate trigger produces a 50ns wide pulse. Data is output on the leading edge and input data is latched on the trailing edge.

Figure 7. Port Registers (2 of 2)

3.6 TRIGGER AND DATA LATCH FUNCTIONALITY

The VX442C provides a number of triggering and data latching capabilities. A functional diagram showing the operation and configuration settings is shown in Figure 8.

Note: A system trigger, latch/hold and port interrupt may occur while configuring a port's trigger function. Therefore, disable triggers and interrupts in the General Status/Control Register and Interrupt Control Register while configuring a port's trigger function. Additionally, the HMODE should be first reset to 00, then set to the desired function.

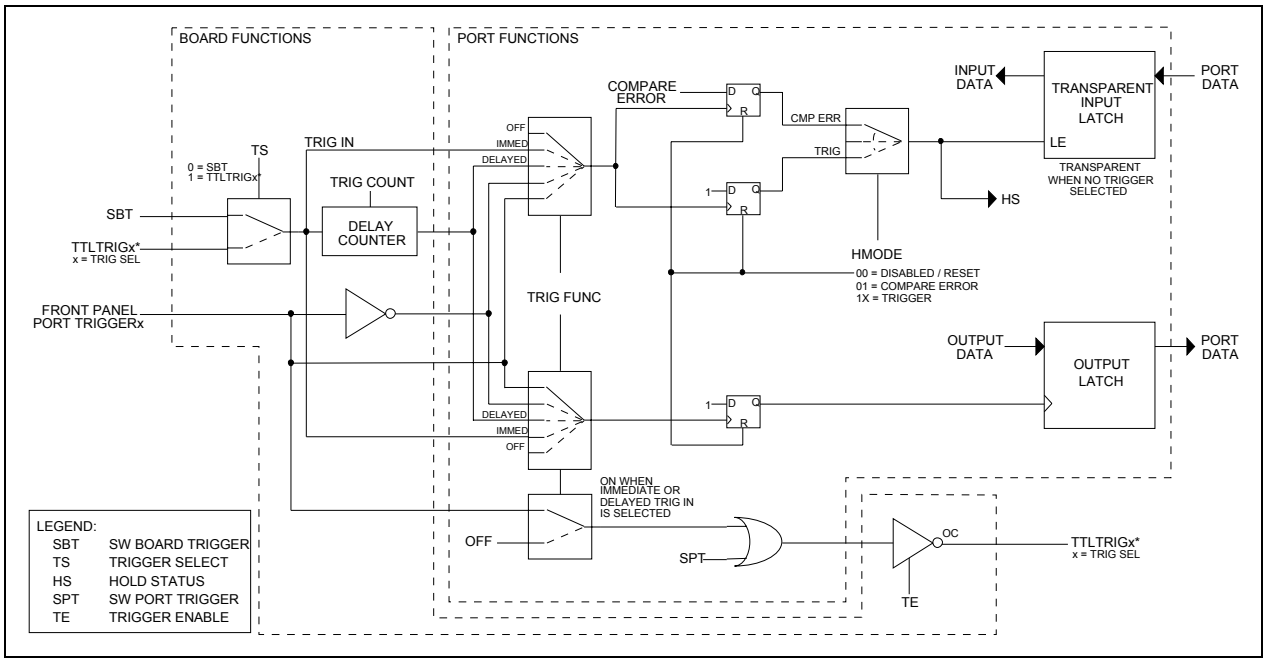


Figure 8. Trigger and Data Latch Functionality

3.6.1 Trigger Modes

A trigger can be caused by a high-to-low transition on the TTLTRGx* line on the VXI P2 connector, by software setting the board trigger (SBT) bit in the General Status/Control Register (Base + $08), or by front panel trigger signal. This TTLTRGx* or SBT may be applied immediately or delayed a programmed amount of time. The delay time is controlled by selecting the desired reference clock period using Trigger Count switches and by programming the Trigger Count value in the General Status/Control Register. The delay time is equal to the Trigger Count value multiplied by the reference clock period as shown in Table II. Note that the Trigger Count must be greater than zero to use any internal trigger. Also the trigger delay uses an asynchronous clock and, therefore, may be up to one reference clock period short depending on the timing of the trigger signal with respect to the clock edge.

Table II. Trigger Count Reference Clock Period Selection

Switch Selection	Reference Clock Period
F	1 µs
E	937.5 ns
D	875 ns
C	812.5 ns
B	750 ns
A	687.5 ns
9	625 ns
8	562.5 ns
7	500 ns
6	437.5 ns
5	375 ns
4	312.5 ns
3	250 ns
2	187.5 ns
1	125 ns
0	invalid

3.6.2 Input Latch and Hold Modes

Input data can be read on-the-fly or be latched upon receipt of a trigger or on the occurrence of a comparison error following a trigger. If the Trigger Function in the Port Status/Control Register is set to an immediate read, the input latch is in a transparent mode (i.e., the data pattern read reflects the current state of the inputs). If the Trigger Function is set to latch on a trigger, the input data is latched and held in accordance with the Hold Mode (HMODE). The Hold Mode determines whether the input data is held on a compare error or on a trigger. See Figure 7 for the possible settings.

3.6.3 Output Latch

Output data may be output to the front panel upon register write or on the occurrence of a trigger. A trigger may originate from a software operation, a VXI P2 TTLTRGx* line, or from the front panel. This capability allows data to be output to the front panel synchronously across all ports and across multiple VXI modules. See Figure 7 for the possible settings.

3.6.4 Data Comparison

When a trigger occurs, the input data is compared to the expected data pattern. The expected data pattern is the pattern that was written to the Port (Output) Data register. Note that this value may be different from the output driver state, since the output drivers may be individually disabled using the Port Enable/Disable Register. The bit positions set to a 1 in the Compare Mask Pattern in the Port Mask Register are ignored during this comparison. If one or more bits do not match, the Compare Status (CMP bit in the General Status/Control Register) is cleared (set to 0) and the bits positions failing the comparison are set to a 1 and saved in a separate register. This "fail bit" pattern can be read by setting the Read Mode (RM bit in the Port Status/Control Register) to a 1, and then reading the Port Data Register.

3.6.5 Interrupts

Each port of the VX442C module is capable of generating an interrupt. An interrupt is generated according to the Hold Mode (HMODE) in the Port Status/Control Register. If "Hold on compare error after trigger" is selected, then an interrupt is generated when a bit error occurs. If "Hold on trigger" is selected, then an interrupt is generated on an immediate trigger or delayed trigger depending on the Trigger Function (TRIG FUNC) selected. Port interrupts are disabled, if "Hold disabled" is selected.

The interrupt level and the interrupt vector/logical address are programmed by writing to the Interrupt Control Register (Base +$0A) as detailed in Figure 6. Interrupts can be completely disabled by setting the interrupt level to 000. The level and vector are used for all interrupts generated by the module to the VXI bus. For VXI compliant interrupts, the interrupt vector/logical address field must be set equal to the logical address assigned to the card. During an interrupt acknowledge cycle, data bits 15 - 8 are $FF and bits 7 - 0 are equal to the value set in the vector/logical address field.

Once an interrupt occurs, the interrupt is released by resetting (i.e., writing binary 00) to the HMODE in the Port Status/Control Register. This Release-On-Register Access (RORA) interrupt acknowledge method allows interrupts to occur on multiple ports and be serviced together or separately. For example, if an interrupt is pending on Port00 and Port05, the host interrupt service routine may service the Port00 interrupt only, by resetting only Port00's HMODE to release its interrupt. The Port05 interrupt will still be pending. Alternatively, the interrupt service routine may process all interrupts together, by continuing the process until Interrupt Pending (IP*) in the Interrupt Control Register goes high. The servicing process is flow charted in Figure 9.

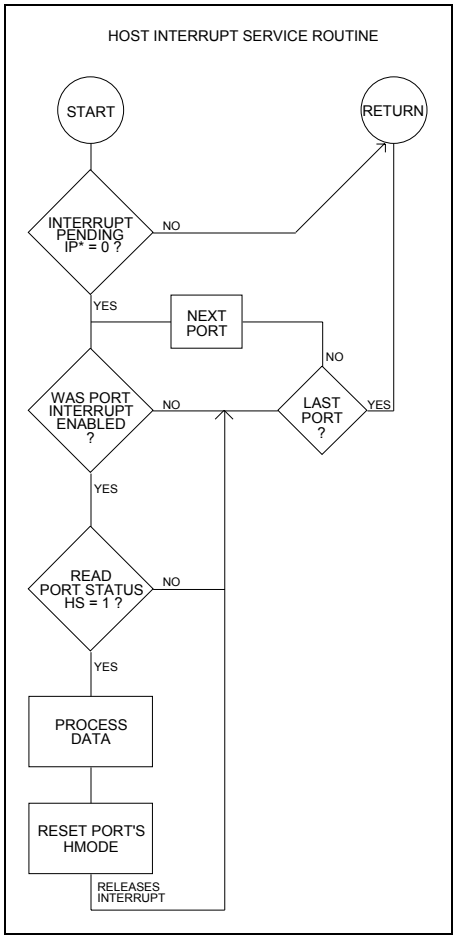


Figure 9. Interrupt Service Program Flow

4.0 OPERATING INSTRUCTIONS

4.1 NORMAL OPERATION

Prior to installation, the module's logical address must be set. The logical address has a range of 0 to 255. Any value within this range is valid, but care should be taken not to set the logical address the same as another module in the system. Position 1 on the switch (marked 128 on the shield) is the most significant bit and has a weighted value of 128 when the switch is in the off position (marked 1 on shield). Position 8 on the switch (marked 1 on the shield) is the least significant bit and has a weighted value of 1 when the switch is in the off position. The sum of the weighted values of all the switches in the off position (marked 1 on the shield) is the module's logical address. The VXI secondary address is the logical address divided by 8.

After installation and power-up, configure the General Status/Control Register to the desired trigger and comparison operation and the Port Status/Control Register to the desired latch, hold, and trigger modes. An example of accessing the various registers is shown below. The VXI Configuration Registers do not require any setup. The module is now ready for normal input/output operations. The typical program flow is shown in Figure 10.

C / Lab Windows Register Access Example

```
static int  port0,cont,ad;

main()
{
int     ad;
int     stat_sel,data_sel,fb_sel,en_sel;
int     statin,datain,fbin,enin;

        ad          = 2;  /*  board Logical Address        */
        port0       = 12; /*  port register                */
        cont        = 8;  /*  general status/control       */
        stat_sel    = 4;  /*  port status/control function */
        data_sel    = 0;  /*  port data function           */
        fb_sel      = 1;  /*  port readback function       */
        en_sel      = 2;  /*  port enable/disable function */

        InitVXIlibrary ();

    /*  Set general control register to port status/control.  */
    /*  Write control and read status port registers.         */
        VXIoutReg (ad, cont, stat_sel);
        VXIoutReg (ad, port0, 0x0000);
        VXIinReg (ad, port0, &statin);

    /*  Set general control register to port enable register. */
    /*  Write and read the enable register.                   */
        VXIoutReg (ad, cont, en_sel);
        VXIoutReg (ad, port0, 0xFF00);
        VXIinReg (ad, port0, &enin);

    /*  Set general control register to port write data and   */
    /*  read feedback registers.                              */
    /*  Write and read the data register.                     */
        VXIoutReg (ad, cont, fb_sel);
        VXIoutReg (ad, port0, 0xAA00);
        VXIinReg (ad, port0, &fbin);

    /*  Set general control register to port write data and   */
    /*  read data registers.                                  */
    /*  Write and read the data register.                     */
        VXIoutReg (ad, cont, data_sel);
        VXIoutReg (ad, port0, 0xAA00);
        VXIinReg (ad, port0, &datain);

        FmtOut("Status = %i\n,Feedback = %i\n",statin,fbin);
        FmtOut("Data = %i\n,Enable = %i\n",datain,enin);
}
```

Figure 10. Typical Program Flow

5.0 MAINTENANCE

5.1 BUILT IN TEST AND DIAGNOSTICS

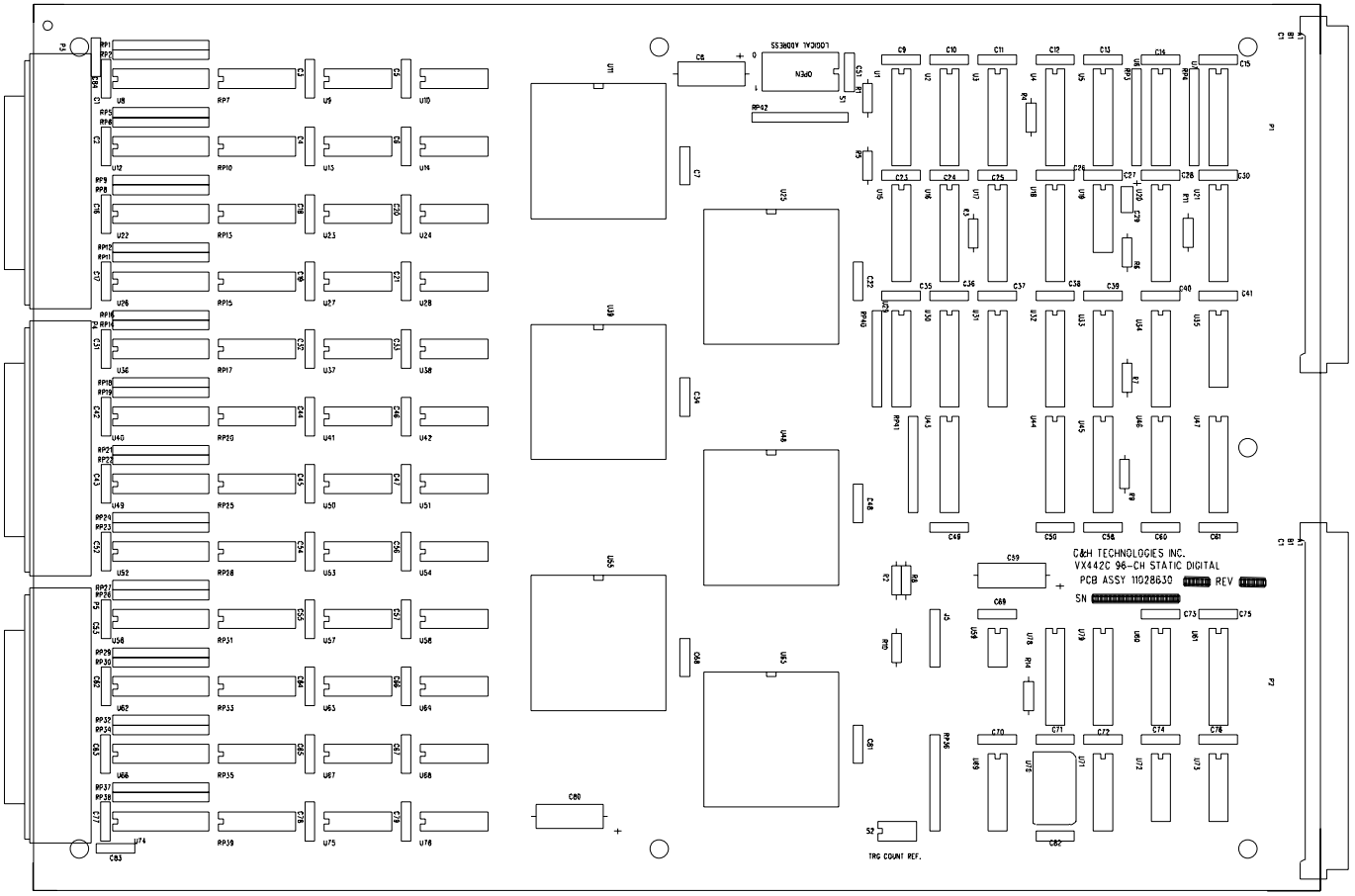
A simple diagnostic routine can be written that uses the read back capability of the modules to insure proper operation up to the driver devices.

5.2 TROUBLE ANALYSIS GUIDE

If a bus error or bus timeout error occurs, verify that the address and mode switch settings are properly set for the system access type. Verify correct program addressing and word size and check the system memory mapping strategy.

If bit errors occur, utilize the modules read back capability to verify the module's internal states. When diagnosing output problems, isolate the module from external loads by removing the connectors. Verify that the input to the output driver matches the output of the driver when it is enabled.

APPENDIX A - BOARD LAYOUT



APPENDIX B - CONNECTORS

PIN	C	B	A
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	-	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	A23	-	-
16	A22	AM0	DTACK*
17	A21	AM1	_
18	A20	AM2	_
19	A19	AM3	_
20	A18	GND	IACK*
21	A17	-	IACKIN*
22	A16	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

Figure B-1. P1 Pin Configuration

PIN	C	B	A
1	-	+5V	-
2	-	GND	-
3	-	-	-
4	-	-	GND
5	-	-	-
6	-	-	-
7	GND	-	-
8	-	-	-
9	-	-	-
10	GND	-	GND
11	-	-	-
12	-	GND	-
13	-	+5V	-
14	-	-	-
15	-	-	-
16	GND	-	GND
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	GND	GND	GND
23	TTLTRG1*	-	TTLTRG0*
24	TTLTRG3*	-	TTLTRG2*
25	GND	-	+5V
26	TTLTRG5*	-	TTLTRG4*
27	TTLTRG6*	-	TTLTRG6*
28	GND	-	GND
29	-	-	-
30	GND	-	MODID
31	-	GND	GND
32	-	+5V	-

Figure B-2. P2 Pin Configuration

PIN	SIGNAL		PIN	SIGNAL
1	TRIG1		40	GND
2	PORT01-7		41	GND
3	PORT01-6		42	GND
4	PORT01-5		43	GND
5	PORT01-4		44	GND
6	PORT01-3		45	GND
7	PORT01-2		46	GND
8	PORT01-1		47	GND
9	PORT01-0		48	GND
10	NO CONNECT		49	GND
11	NO CONNECT		50	GND
12	PORT02-0		51	GND
13	PORT02-1		52	GND
14	PORT02-2		53	GND
15	PORT02-3		54	GND
16	PORT02-4		55	GND
17	PORT02-5		56	GND
18	PORT02-6		57	GND
19	PORT02-7		58	GND
20	TRIG2		59	GND
21	GND		60	PORT03-0
22	GND		61	PORT03-1
23	GND		62	PORT03-2
24	GND		63	PORT03-3
25	GND		64	PORT03-4
26	GND		65	PORT03-5
27	GND		66	PORT03-6
28	GND		67	PORT03-7
29	GND		68	TRIG3
30	GND		69	NO CONNECT
31	GND		70	TRIG0
32	GND		71	PORT00-7
33	GND		72	PORT00-6
34	GND		73	PORT00-5
35	GND		74	PORT00-4
36	GND		75	PORT00-3
37	GND		76	PORT00-2
38	GND		77	PORT00-1
39	GND		78	PORT00-0

Figure B-3. J1 Connector

PIN	SIGNAL		PIN	SIGNAL
1	TRIG5		40	GND
2	PORT05-7		41	GND
3	PORT05-6		42	GND
4	PORT05-5		43	GND
5	PORT05-4		44	GND
6	PORT05-3		45	GND
7	PORT05-2		46	GND
8	PORT05-1		47	GND
9	PORT05-0		48	GND
10	NO CONNECT		49	GND
11	NO CONNECT		50	GND
12	PORT06-0		51	GND
13	PORT06-1		52	GND
14	PORT06-2		53	GND
15	PORT06-3		54	GND
16	PORT06-4		55	GND
17	PORT06-5		56	GND
18	PORT06-6		57	GND
19	PORT06-7		58	GND
20	TRIG6		59	GND
21	GND		60	PORT07-0
22	GND		61	PORT07-1
23	GND		62	PORT07-2
24	GND		63	PORT07-3
25	GND		64	PORT07-4
26	GND		65	PORT07-5
27	GND		66	PORT07-6
28	GND		67	PORT07-7
29	GND		68	TRIG7
30	GND		69	NO CONNECT
31	GND		70	TRIG4
32	GND		71	PORT04-7
33	GND		72	PORT04-6
34	GND		73	PORT04-5
35	GND		74	PORT04-4
36	GND		75	PORT04-3
37	GND		76	PORT04-2
38	GND		77	PORT04-1
39	GND		78	PORT04-0

Figure B-4. J2 Connector

PIN	SIGNAL		PIN	SIGNAL
1	TRIG9		40	GND
2	PORT09-7		41	GND
3	PORT09-6		42	GND
4	PORT09-5		43	GND
5	PORT09-4		44	GND
6	PORT09-3		45	GND
7	PORT09-2		46	GND
8	PORT09-1		47	GND
9	PORT09-0		48	GND
10	NO CONNECT		49	GND
11	NO CONNECT		50	GND
12	PORT10-0		51	GND
13	PORT10-1		52	GND
14	PORT10-2		53	GND
15	PORT10-3		54	GND
16	PORT10-4		55	GND
17	PORT10-5		56	GND
18	PORT10-6		57	GND
19	PORT10-7		58	GND
20	TRIG10		59	GND
21	GND		60	PORT11-0
22	GND		61	PORT11-1
23	GND		62	PORT11-2
24	GND		63	PORT11-3
25	GND		64	PORT11-4
26	GND		65	PORT11-5
27	GND		66	PORT11-6
28	GND		67	PORT11-7
29	GND		68	TRIG11
30	GND		69	NO CONNECT
31	GND		70	TRIG8
32	GND		71	PORT08-7
33	GND		72	PORT08-6
34	GND		73	PORT08-5
35	GND		74	PORT08-4
36	GND		75	PORT08-3
37	GND		76	PORT08-2
38	GND		77	PORT08-1
39	GND		78	PORT08-0

Figure B-5. J3 Connector

NOTES

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