U S E R ' S M A N U A L

100MHZ SIGNAL DISTRIBUTION M-MODULE

MODEL MA210

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA210 100MHz Signal Distribution M-Module (Part Number 11028800, Rev. B or higher). This mezzanine module is designed to interface within any M-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on low level register accesses, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction on using the higher level interface provided by the driver.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The MA210 provides distribution of clock signals to other devices. The module accepts two analog input signals and provides TTL and ECL distribution. The input signals are passed through high speed comparators that convert the analog level to a digital signal. The digital signals are individually buffered to provide the TTL and ECL outputs.

The module is physically implemented on a double-wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The MA210 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the MA210 to be used in VXI, VME, PCI, cPCI and many other system architectures.

1.1 PURPOSE OF EQUIPMENT

The MA210 can be used in a wide variety of applications including functional verification of digital systems, signal simulation, design verification, and research and development that require the distribution of clock and timing signals.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- Two Input Channels
- 100MHz Maximum Frequency
- Each input channel supports 1 ECL output and 4 TTL outputs
- Input A or B can be configured to support 8 TTL outputs [1]
- Input High and Low levels are individually programmed for each input
- Trigger input with software programmable threshold
- Non-volatile potentiometers retain setting when power is off
- Switch settings allow full operation at factory set levels (no software programming required)
- M-Triggers supported (source for input channels or trigger output)

[1] Input A or B can drive either four TTL outputs or all eight TTL outputs. If Input A is configured to drive eight TTL outputs, then Input B drives no TTL outputs and vice versa. The ECL output of each input signal is not affected.

1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption (power is shared by both M-module connectors)	+5V +12V -12V	1200 50 400	mA mA mA
Input Voltage (INA, INB, TRIGIN)	no damage	±10	Vrms

AC CHARACTERISTICS

		Limit			
Parameter	**Conditions**	**Min**	**Typ.**	**Max**	**Units**
Common Input Characteristics					
Voltage Range		-5.0		+5.0	V
Input Impedance	Switch = 50Ω Switch = Hi-Z	48 10K	50 10.3K	52 10.6K	Ω Ω
Level Adjust Resolution	8 bit		39		mV
Threshold Level Accuracy	Input Impedance = 50Ω Input Impedance = Hi-Z	±7% + 150mV ±10% + 150mV			% + mV % + mV
Frequency	Input Impedance = 50Ω Input Impedance = Hi-Z	0 0		100 50	MHz MHz
Width		3		∞	ns
INA/INB Input Characteristics					
High Threshold Level Range[1]	Software programmable	-5.0		+5.0	V
Low Threshold Level Range[1]	Software programmable	-5.0		+5.0	V
Fixed Factory Default Levels	High Level Low Level		+2.15 +1.85		V V
Trigger Input Characteristics					
Input Threshold	Software programmable	-5.0		+5.0	V
Fixed Factory Default Level			+2.0		V
TTL Output Characteristics					
Impedance[2]			12.5		Ω
Output Levels	Load = 50Ω, V_{OL} V_{OH}	 2.4		0.5	V V
Propagation Delay	INA or INB to TTLOUT MTRIG to TTLOUT		14 24	21 30	ns ns
Skew	same input, adjacent outputs [3]		0.5	3.0	ns
ECL Output Characteristics					
Type	10K Series ECL				
Termination	499Ω pull downs (-5.2V) on both lines				
Propagation Delay	INA or INB to ECLOUT MTRIG to ECLOUT		5 14	7 21	ns ns
Skew	same input, ECLOUT1 to ECLOUT2			50	ps

AC CHARACTERISTICS (continued)

Trigger Output Characteristics					
Impedance			50		Ω
Output Levels	Load = 50Ω, V_{OL} V_{OH}	 2.1		0.4	V V
Width		3		∞	ns
Propagation Delay	TRIGIN to TRGOUT		14	21	ns
Skew	TRGOUT1 to TRGOUT2			1.0	ns

Notes:
1. The high level must be higher than the low level for proper operation.
2. Four output drivers with 50Ω source impedance each are used in parallel.
3. Adjacent outputs are TTLOUT1 to TTLOUT2, TTLOUT3 to TTLOUT4, TTLOUT5 to TTLOUT6, or TTLOUT7 to TTLOUT7.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for double-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 4.182" (106.2 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for double-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	not supported
DMA:	not supported
Triggers:	not supported
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00D2_{16}$ (210 dec.)

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA210 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.

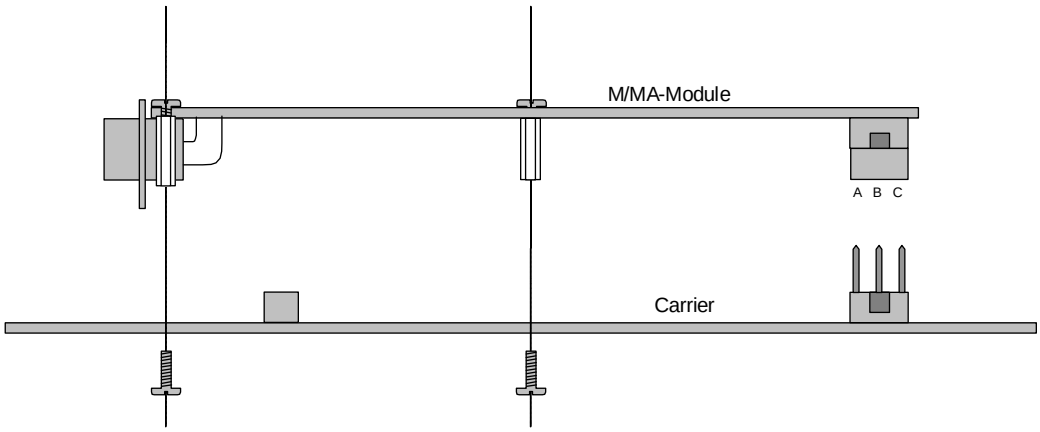

Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

The MA210 uses high speed comparator and ECL logic to provide low propagation delay signal distribution of two input signals. Each input signal is buffered and distributed to TTL and ECL outputs. A TRGIN function provides limited distribution for a third input. The module can be configured to handle a variety of input signals. A simplified block diagram is shown in Figure 2.

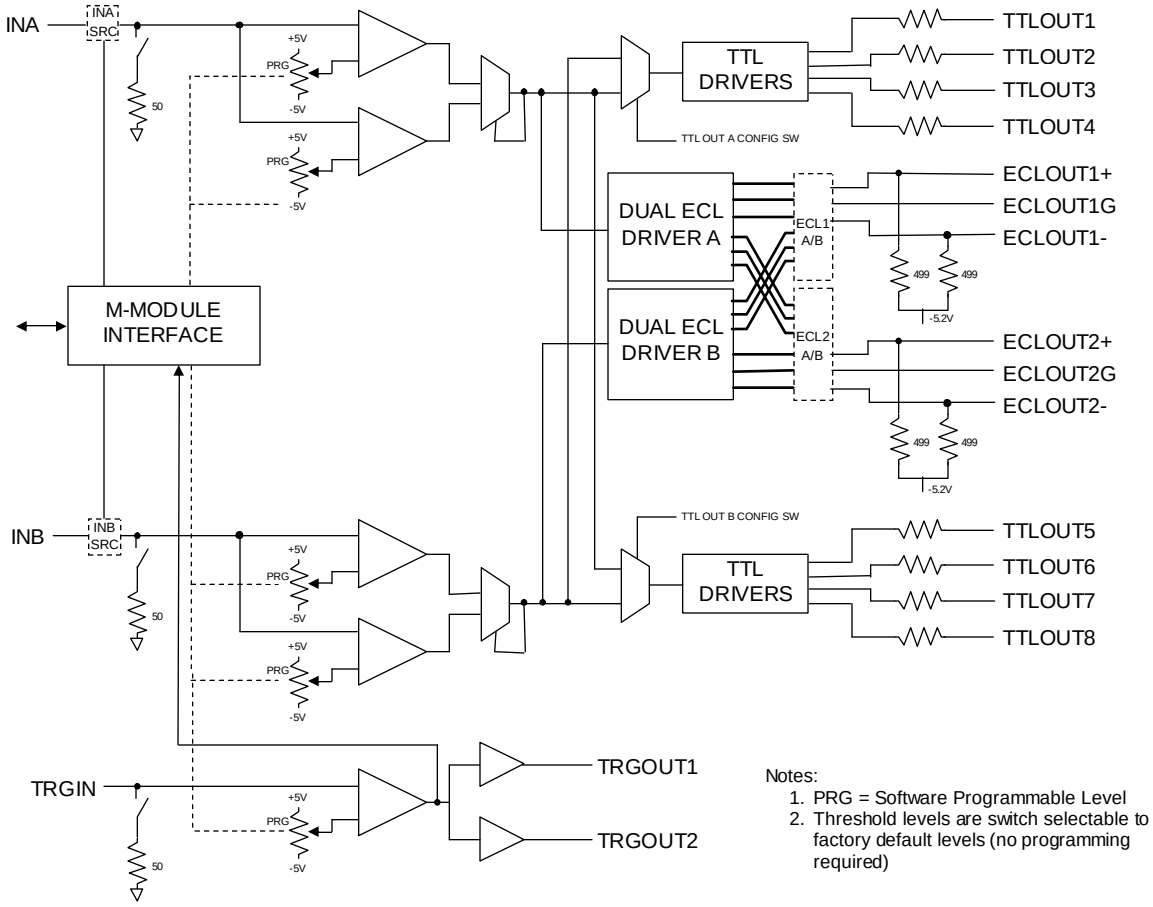

Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the MA210 and the carrier module. The interface is an asynchronous 16-bit data bus. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules. The interface also permits the mapping of M-module triggers as sources for the two standard inputs or as a destination for the TRGIN input signal.

3.1.2 Input Comparators

Input comparators provide high speed analog to digital conversion with programmable high and low levels. The comparators are configured to provide a hysteresis window for the input signal. As an input signal transitions from low to high, it must exceed the high threshold level to produce a high at the window comparator output. As an input signal transitions from high to low, it must fall below the low threshold level to produce a low at the window comparator output.

The comparator threshold levels can be either programmable or set to a factory default value. A hardware configuration switch provides this selection. The programmable threshold levels are set by programming a group of digitally programmable potentiometers. These potentiometers are non-volatile so they retain their setting even when power to the module is off.

The source of the input comparators is switch selectable as either the front panel input connectors or the internal M-module trigger lines. Input impedance is also switch selectable as either 50 Ohms or HI-Z.

3.1.3 TTL Drivers

Eight TTL outputs provide TTL compatible signal distribution of the input signals. Each input can be distributed to four TTL outputs or the module can be configured to distribute a single input to all eight TTL outputs.

Each TTL output consists of four output buffers in parallel. The output source impedance of each individual driver is 50Ω, thus providing an overall output source impedance of 12.5Ω that can drive TTL compatible logic levels into a 50Ω load.

3.1.4 ECL Drivers

Two ECL outputs provide ECL compatible signal distribution of the inputs. The source (INA or INB) of the ECL signals can be selected for each ECL output. The differential ECL outputs are terminated through 499Ω resistors to -5.2V.

3.1.5 Trigger Input Comparator & Distribution

The TRGIN function provides limited distribution for a third input. The TRGIN signal is distributed to two TRGOUT connectors (internal PCB mounted) and can programmatically be distributed to the M-Module trigger lines. The input comparator logic is similar to the standard inputs, however a hysteresis window in not provided. Instead, a single threshold level can be programmed or set to a factory default level as selected by a hardware configuration switch.

3.2 HARDWARE CONFIGURATION

The MA210 contains a variety switches that select the various configurations of the module including: input impedance of the inputs, the output configuration of the inputs, the threshold levels of inputs, and the source of the inputs. The switches are only accessible with the module removed from the carrier and are located as shown in Figure 3.

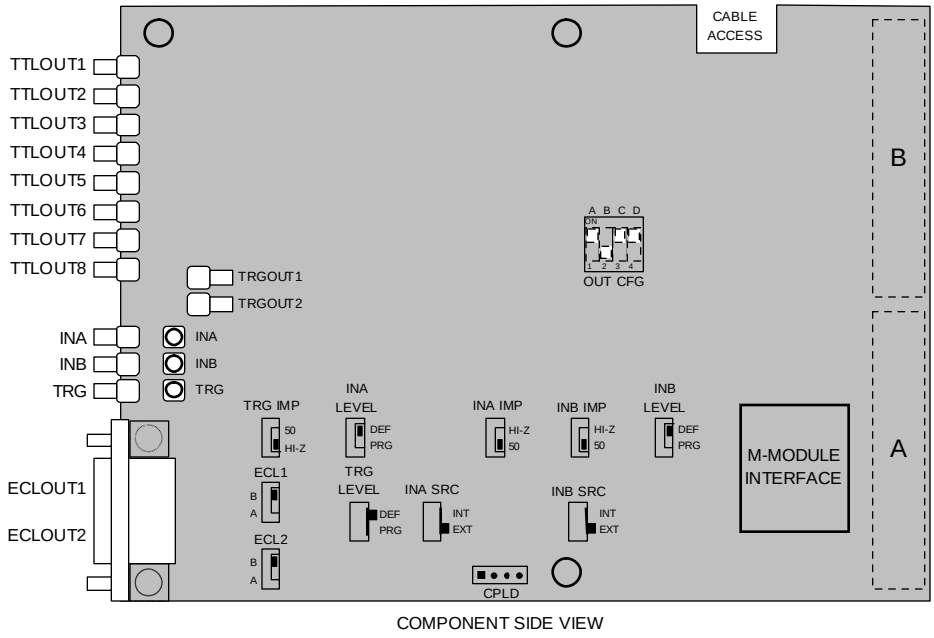

Figure 3. MA210 Hardware Configuration Switches

INA IMP Switch This switch selects the input impedance of the input A signal to be 50Ω or high impedance (~10KΩ).

INB IMP Switch This switch selects the input impedance of the input B signal to be 50Ω or high impedance (~10KΩ).

TRG IMP Switch This switch selects the input impedance of the trigger input signal to be 50Ω or high impedance (~10KΩ).

INA SRC Switch This switch selects whether the INA signal come from the internal M-module trigger input or from the external front panel connector.

INB SRC Switch This switch selects whether the INB signal come from the internal M-module trigger input or from the external front panel connector.

INA LEVEL Switch This switch selects whether the input A threshold levels are software programmable or set to the fixed factory default levels of high = +2.15V, low = +1.85V (no programming required).

INB LEVEL Switch This switch selects whether the input B threshold levels are software programmable or set to the fixed factory default levels of high = +2.15V, low = +1.85V (no programming required).

TRG LEVEL Switch This switch selects whether the trigger input threshold level is software programmable or set to the fixed factory default level of +2.00V (no programming required).

ECL1 Switch This switch selects whether the ECL1 signals are from INA or INB.

ECL2 Switch This switch selects whether the ECL2 signals are from INA or INB.

OUT CFG Switch These switches configure the source of the TTL outputs and select the operational mode of the logic.

TTL Output 1-4	IN CFG Switch A
Input A Drives Outputs (Normal)	OFF
Input B Drives Outputs	ON

TTL Output 5-8	IN CFG Switch B
Input B Drives Outputs (Normal)	OFF
Input A Drives Outputs	ON

Operational Mode	IN CFG Switch D
Normal	OFF
Special Mode	ON

Note: Switch C is not used.

3.3 INPUT/OUTPUT SIGNALS

The front panel input/output signals are as shown in Figure 4 and are briefly described below. MMCX jack receptacles are used for the TRG, INB, INA, and TTLOUT signals and a 9-pin DSUB plug provides connection to the ECLOUT1 and ECLOUT 2 signals. In addition to the front panel connectors, internal MMCX connectors are provided INA, INB, TRG, TRGOUT1, and TRGOUT2. These connectors facilitate integration with other M-modules. Cable access is provided through a notch on one side the board (see Figure 3). The internal INA, INB, and TRG connectors are straight vertical connectors and require a right-angle mating connector. The internal TRGOUT1 and TRGOUT2 connectors are right-angle connectors and a straight mating connector is recommended.

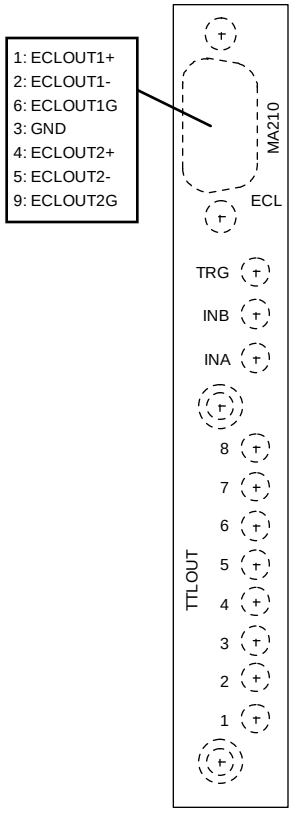

Figure 4. Front Panel

ECLOUT1+ & ECLOUT1+ These signal contacts are the ECL output positive signals.

ECLOUT2- & ECLOUT2- These signal contacts are the ECL output negative signals.

ECLOUT1G & ECLOUT2G These signal contacts are the ECL output ground signals.

TRG This MMCX connector is the TRGIN signal input. TRGIN can be input through this connector or through the internal PCB MMCX connector.

INB This MMCX connector is the INB signal. INB can be input through this connector or through the internal PCB MMCX connector.

INA This MMCX connector is the INA signal. INA can be input through this connector or through the internal PCB MMCX connector.

TTLOUT1-8 These MMCX connectors are the TTL output signals.

TRGOUT1 & TRGOUT2 These internal PCB mounted MMCX connectors are the distributed TRGOUT signals.

CAUTION: To avoid MMCX connector breakage, mating connectors must be inserted and removed using forces in-line with the connector barrel. Avoid side to side pressure.

3.4 IDENTIFICATION AND CONFIGURATION REGISTERS

3.4.1 I/O Registers

There are a variety of registers used to configure and control the MA210 module. These registers are located in the IOSpace. The address map of the registers is shown in Table I. Details of the registers are provided in Figure 5.

Table I. I/O Address Map/Command Summary

IO REG. (HEX)	REGISTER DESCRIPTION
00	Configuration
02	Input A Threshold Level Control
04	Input B Threshold Level Control
06	Trigger Threshold Level Control

MA210 Reg. 00 — **Configuration**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write											TRGO		SRCB		SRCA	
Read											TRGO		SRCB		SRCA	

SRCA ⇨ Input A Source
- 0 0 Front Panel
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 not used

SRCB ⇨ Input B Source
- 0 0 Front Panel
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 not used

TRGO ⇨ Input Trigger Output
- 0 0 none (internal SMA connectors only)
- 0 1 M-Trigger A
- 1 0 M-Trigger B
- 1 1 Both M-Trigger A & B

Note: The INA SRCA and/or INB SRC switches must be configured to INT to use the M-Triggers as inputs.

Figure 5. MA210 I/O Registers

MA210
Reg. 02

Input A Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELA	-	DIA	CLKA
Read													SELA	-	DIA	CLKA

SELA ⇨ Select Input A Threshold Level potentiometer (1 = active, 0 = inactive)
DIA ⇨ Data input signal to Input A Threshold Level potentiometer
CLKA ⇨ Clock signal to Input A Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Section 4.1 for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The INA LEVEL switch must be set to PRG for the programmed threshold to take affect.

MA210
Reg. 04

Input B Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELB	-	DIB	CLKB
Read													SELB	-	DIB	CLKB

SELB ⇨ Select Input B Threshold Level potentiometer (1 = active, 0 = inactive)
DIB ⇨ Data input signal to Input B Threshold Level potentiometer
CLKB ⇨ Clock signal to Input B Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Section 4.1 for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The INB LEVEL switch must be set to PRG for the programmed threshold to take affect.

MA210
Reg. 06

Trigger Threshold Level Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													SELT	-	DIT	CLKT
Read													SELT	-	DIT	CLKT

SELT ⇨ Select Trigger Threshold Level potentiometer (1 = active, 0 = inactive)
DIT ⇨ Data input signal to Trigger Threshold Level potentiometer
CLKT ⇨ Clock signal to Trigger Threshold Level potentiometer

Notes:
1. These bits directly control the 3-wire serial interface to the potentiometer. See Section 4.1 for programming details. A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit.
2. The TRG LEVEL switch must be set to PRG for the programmed threshold to take affect.

Figure 5. MA210 I/O Registers (continued)

3.4.2 Module Identification

The MA210 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.2. Data can not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

Table II. M-Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00D2 (210 dec.)
2	Revision Number[1]	0000
3	Module Characteristics[2]	1E68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[3]	FFE1 (MA210)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	1 = trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE1_{16}$ = C&H specified VXI model code for MA210

4.0 OPERATION

The MA210 is a register-based instrument that is controlled through the I/O registers described in Section 3.4.1. The module can also be operated without any software control, if the default input levels are acceptable (see Section 3.2 for switch details). The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

4.1 PROGRAMMING THRESHOLD LEVELS

The input threshold levels are programmed by writing bit values to the Input Threshold Level Control registers (Reg. 00 and 02). A programmed value 00_{16} = -5.0V and FF_{16} = +5.0V. The resolution is 39mV per bit. The CLKx and DIx bits directly control the serial bus signals connected to the digital potentiometer. The SELx bit must be set to 1 at least one write cycle before writing a 1 to the CLKx bit. The bits are written by sequentially writing to the control registers according to Figure 6.

Channel Input Programming:

→ Bits are written in this direction (Bit 0 is first bit written, Bit 16 is last bit written)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	MSB				Input X Low Threshold Level			LSB	MSB			Input X High Threshold Level				LSB

X ⇨ Don't Care

Trigger Input Programming:

→ Bits are written in this direction (Bit 0 is first bit written, Bit 16 is last bit written)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	X	X	X	X	X	X	X	MSB			Trigger Input Threshold Level				LSB

X ⇨ Don't Care

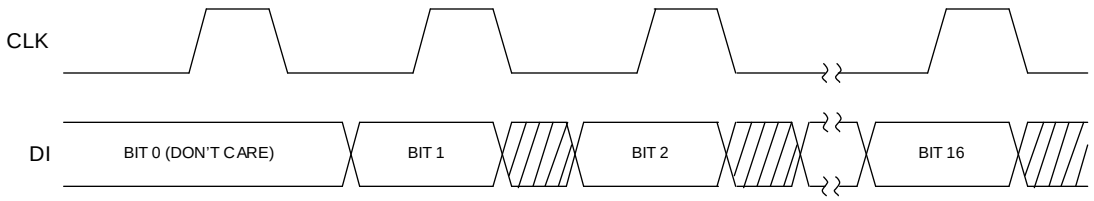

Figure 6. Potentiometer Serial Programming

4.2 ID PROM

Refer to 3.4.2 for a description of the ID PROM's function and contents. Reading data from the ID PROM involves writing and reading a register in a sequential manner. Data can not be written to the PROM. Figure 7 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_prbyte (addr, id_addr);
  read_prbyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_prbyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*-------------------------------------------------------------------------*/
int write_prbyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_prbit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_prbit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*-------------------------------------------------------------------------*/
int write_prbit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------------*/
int read_prbyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_prbit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-------------------------------------------------------------------------*/
int read_prbit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 7. ID PROM Access Routine

APPENDIX A: CONNECTORS

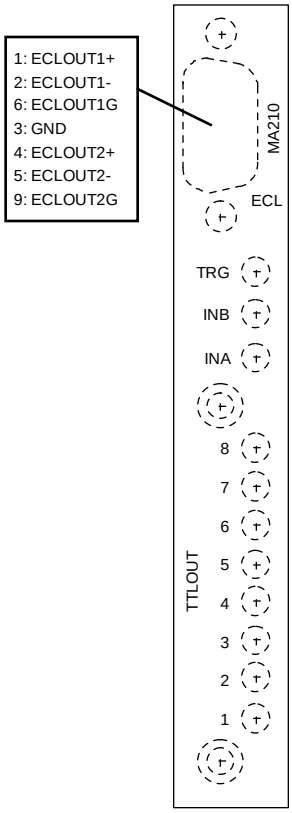

Figure A- 1 Front Panel Connector

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure A- 2 M-Module Interface

N O T E S:

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