U S E R ' S M A N U A L

50MHZ PULSE GENERATOR M-MODULE

MODEL MA204

Document Part No: 11028454

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NOTE

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA204 50MHz Pulse Generator MA-Module (Part Number 11028450). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The MA204 is a fully programmable 50MHz pulse generator that allows the generation of precisely timed pulses of programmable pulse width, delay, amplitude, and frequency. Operational modes include single, continuous, and burst functions along with double pulse capability. Extensive trigger and gating logic provides comprehensive control of pulse timing. The internal base clock can be locked to an external reference clock. The -0001 version provides fine 100ps control resolution of the pulse width and pulse delays. The lower cost -0002 version provides only 5ns control resolution.

The module is physically implemented on a single wide MA-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The MA204 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the MA204 to be used in VXI, VME, PCI, cPCI and many other system architectures.

1.1 PURPOSE OF EQUIPMENT

The MA204 can be used in a wide variety of applications including functional verification of digital systems, signal simulation, design verification, and research and development.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- 50MHz frequency
- -2V to +7V pulse amplitude
- Single or continuous pulsing
- Single pulse or pulse pair
- Programmable rise/fall time
- External triggering
- Asynchronous or synchronous gating
- Programmable burst from 2 to >4B pulses
- Pulse Out & Sync Out enable/disable
- Internal clock can be disciplined to an external reference

1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	-0001 (with fine delay capability)		
	+5V	1.3	A
	+12V	200	mA
	-12V	200	mA
	-0002 (without fine delay capability)		
	+5V	200	mA
	+12V	170	mA
	-12V	180	mA
Input Voltage (FPSIGA & FPSIGB)	no damage	±14	Vrms

AC CHARACTERISTICS

Parameter	Conditions	Limit Min	Typ.	Max	Units
Dynamic Performance					
Pulse Period					
- Range	internal clock triggering	20e-9		5.2	sec
	external triggering	20e-9		∞	sec
- Programming Step Size			100		ps
- Resolution [1]	Period: 20 to 79.9ns		100	100	ps
	80 to 159.9ns		80	160	ps
	160 to 319.9ns		160	320	ps
	320 to 639.9ns		320	640	ps
	640 to 1279.9ns		0.640	1.28	ns
	1280 to 4999.9ns		1.28	2.56	ns
	≥5µs		5	5	ns
- Accuracy [2]	internal clock	±(0.01% + 100ps)			% + ps
Pulse Width					
- Range [3]		10e-9		5.2	Sec
- Resolution	-0001 version		100		ps
	-0002 version		5		ns
- Accuracy [2, 4]	internal clock	±(0.01% + 2ns)			% + ns
Pulse & Pulse Pair Delay	from Sync Out				
- Range		20e-9		5.2	sec
- Resolution	-0001 version		100		ps
	-0002 version		5		ps
- Accuracy [2, 4]	internal clock	±(0.01% + 2ns)			% + ns

AC CHARACTERISTICS (continued)

Parameter	Conditions	Limit Min	Typ.	Max	Units
Pulse Output Characteristics					
Output Voltage Range	$R_L = \infty$	-2.0		+7.0	V
Output Impedance	Software programmable		3		Ω
			50		Ω
Resolution			25		mV
Accuracy			±(2.0% + 100mV)		% + mV
Output Current	Source			50	mA
	Sink			50	mA
Short Circuit Current	Static		±35		mA
	Dynamic		±100		mA
Rise/Fall Time	Software programmable, $R_L = \infty$	1.0		2.5	V/ns
Input Characteristics (FPSIGA & FPSIGB)					
Input Impedance	Switch selectable	36	56	75	Ω
		55	82	110	Ω
		120	180	240	Ω
			>100K		Ω
Input Threshold	Switch selectable	-2.2	-2.0	-1.8	V
		-0.2	0	+0.2	V
		+1.0	+1.2	+1.4	V
		+1.6	+1.8	+2.0	V
Frequency		0		50	MHz
Pulse Width		10		∞	ns
Sync Out Characteristics					
Timing	Time to un-delayed output pulse				
	-0001 version	12	14	16	ns
	-0002 version	2	4	6	ns
	Time from external trigger	50		80	ns
Output Impedance	Switch selectable		3		Ω
			50		Ω
Amplitude	Switch selectable, $R_L = \infty$		5.0		V
			9.0		V
Output Current	source			50	mA
	sink			50	mA
Short Circuit Current	Static		±35		mA
	Dynamic		±100		mA
Rise/Fall Time	Fixed, $R_L = \infty$	2200	2500	2800	V/µs
Pulse Width	period < 80ns	10	15	20	ns
	period ≥ 80ns	40	60	80	ns

Notes:

1. In general, the resolution is 100ps when programming a period less than 5µs; however, there are some areas that have less resolution as specified for the various ranges. See 4.1.2.3 for further details.
2. The percent accuracy can be improved by disciplining the internal clock to an external precision 10MHz reference clock. The internal clock accuracy will discipline in about 10 minutes to within one decade of the external reference, up to 10-8 accuracy.
3. For pulse periods < 40ns, pulse width = ½ period. For periods ≥ 40ns the minimum pulse width = 15-30ns. See 4.1.2.4 for further details.
4. Use of the calibration register can improve the pulse width and pulse delay accuracy.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	Input/Output Trig A and Trig B
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00CC_{16}$ (204 dec.)

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA204 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.

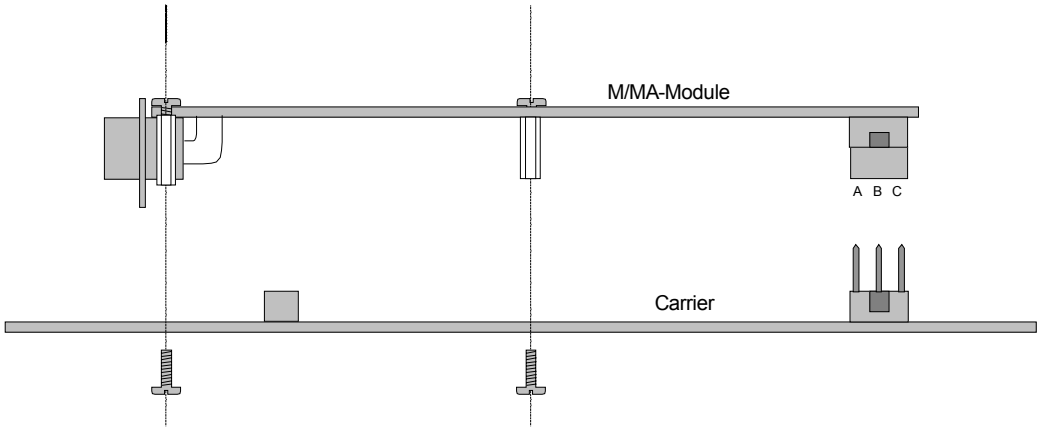

Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

The MA204 utilizes programmable gate array logic, a microcontroller, digital/analog converters, pin driver devices, and variety of other digital and analog electronics to provide the pulse generation function. Register-based commands are received through the M-Module interface and acted upon either directly by the pulse generation logic or the microcontroller. In many cases, the microcontroller translates the register data into appropriate DAC or programmable clock values to produce the desired functionality. A simplified block diagram is shown in Figure 2.

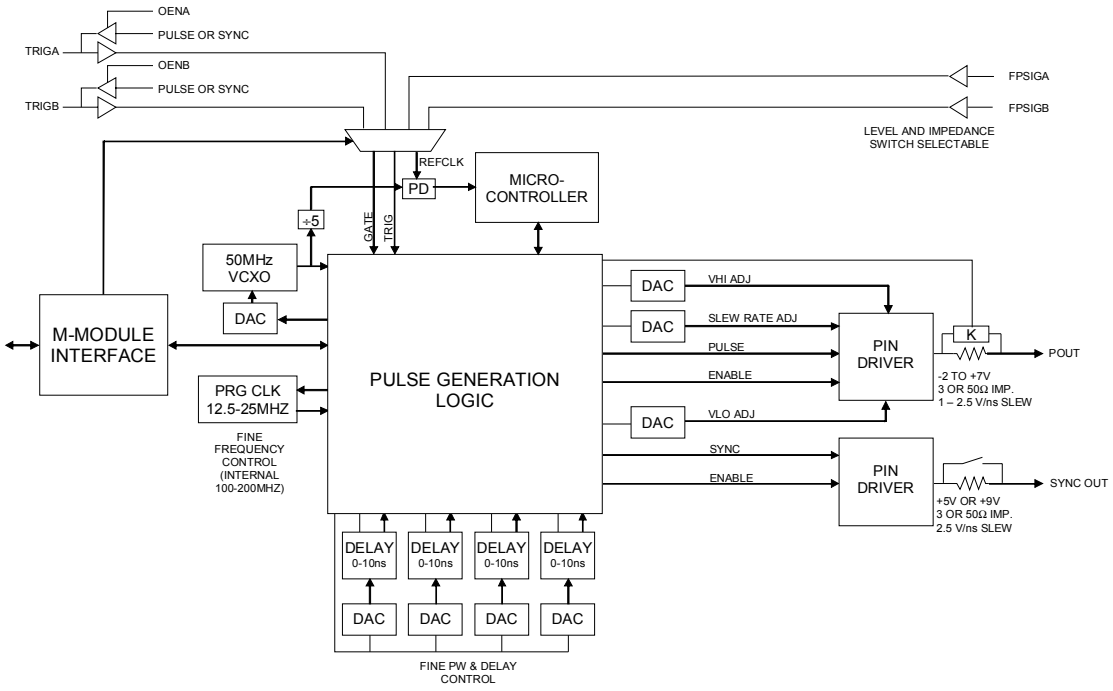

Figure 2. Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the MA204 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt and trigger capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

3.1.2 Pulse Generation Logic

The pulse generation logic provides the main control and generation of the raw pulse. It contains the user programmable control and status registers, the delay lock loop elements for precise clock

control, the interface logic for the microcontroller and other functions, and numerous counters and control logic elements for the pulse formatting functions.

3.1.3 Microcontroller

The microcontroller performs extensive calculations to determine the correct coarse counter and fine delay values for the different points of the generated pulse. The DACs are programmed through the pulse generation logic via a serial interface to set the appropriate fine delay values and pin driver amplitude and slew rate. New values are computed anytime a user modifies a user register.

3.1.4 Programmable Clock

The programmable clock produces a variable frequency clock that is used by the pulse generation logic to produce the desired pulse(s). The programmable clock produces a variable 12.5MHz to 25MHz output clock that is used by the pulse generation logic to control the pulse period, delays, and pulse width. The output frequency is set by the microcontroller based on the desired pulse repetition rate. The programmable clock allows very small (100ps) adjustments in the pulse repetition rate.

3.1.5 VCXO

The voltage controlled oscillator (VCXO) provides the base clock for the module. Even though the internal VCXO is fairly accurate and stable on its own, it can also be disciplined to a high precision 10MHz external clock, if one is available.

3.1.6 Delays

The delays provide the fine resolution control of the pulse delay and pulse width. They are controlled by the microcontroller through the DACs and interface closely with the pulse generation logic. The delays are only used on the -0001 version.

3.1.7 Pin Drivers

The pin driver provides the output voltage, current, and slew rate of the output pulse and Sync Out signals.

3.1.8 Front Panel Input Signals

Two front panel trigger signals are provided for trigger, gate, or clock reference control from an external source. The inputs have switch selectable input impedance and threshold level control.

3.1.9 Backplane Trigger Signals

Two backplane M-module trigger signals are provided. As inputs, these signals can be used for external control of the trigger, gate, or clock reference. As outputs, they can be used to output the pulse and Sync Out signals. To utilize this feature, the M-Module carrier must support triggers (third row on M-module interface). Trigger operation differs depending on the carrier, see your carrier's documentation for details.

3.2 OPERATIONAL MODES

The MA204 can be configured for many different operating modes. In order to fully understand the operation, it is important to have a clear understanding of the terminology used and relationship of the various signals as shown in Figure 3.

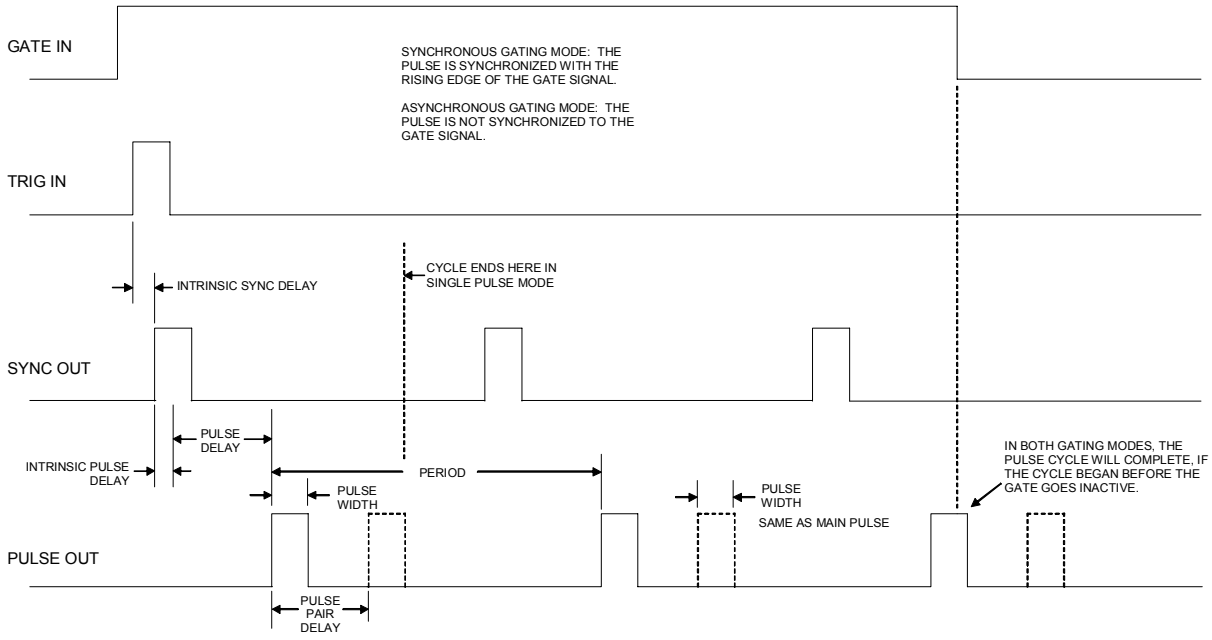

Figure 3. Pulse Terms and Relationships

3.2.1 Pulse Period (Repetition Rate)

The pulse period of the output pulse can be controlled internally using the pulse period register or externally using an external trigger signal.

3.2.2 Pulse Width

The width of the output pulse can be controlled internally using the pulse width register or externally using an external trigger signal.

3.2.3 Pulse Delay and Pulse Pair Delay

The time from the Sync Out signal to the first output pulse and to the second (Pulse Pair) pulse, if enabled, is programmable using the pulse delay and pulse pair delay registers.

3.2.4 Single Pulse or Pulse Pair

The output pulse can be either a single or a double pulse. In Pulse Pair (double pulse) mode, the widths of both pulses are the same. The time from Sync Out to the first pulse and the time from Sync Out to the second pulse are separately programmable.

3.2.5 Run Modes

There are four run modes: single, continuous, burst, and follow trigger. In all cases, except follow trigger, the output pulse can be a single pulse or a pulse pair. The run event can be initiated by software or an external trigger. Single pulse mode produces one pulse (or pulse pair) for each software or trigger signal. Continuous mode continues pulsing until software disables the run. Burst mode allows a preset number of pulses to be produced. In the follow trigger mode, the output pulse follows both the pulse width and period of the trigger input. Gating operations are allowed in all modes.

3.2.6 Pulse Output

The amplitude of the output pulse is programmable using the high and low level amplitude registers. The high level of the pulse and the low level of the pulse are controlled separately. The output can be enabled or disabled (placed in a high-impedance state) and the output impedance (3Ω or 50Ω) and polarity (active-high or active-low) are programmable.

3.2.7 Sync Out

The Sync Out signal, which indicates the start (T_0) of the pulse generation internal timing, can be enabled or disabled (placed in a high-impedance state) and its polarity (active-high or active-low) is programmable. The output impedance (3Ω or 50Ω) is switch selectable.

3.2.8 External Trigger

An external signal can be used to control the pulse repetition rate, instead of the internal counter. Either the positive going or negative going transition can be used. Additionally, the output pulse can follow the pulse width and period of the trigger input signal.

3.2.9 External Gate

The module can be configured to enable pulsing only during the presence of an external signal. The gate operation can be asynchronous or synchronous (see 4.1.6 for details). The external gate can be active-high or active-low.

3.2.10 External Reference Clock

An external 10MHz signal can be used to discipline the internal clock. The internal clock will discipline in about 10 minutes to within one decade of the external reference, up to 10^{-8} accuracy. Software register bits allow enabling the disciplining operation and provide status of the state of the reference and the internal clock.

3.3 HARDWARE CONFIGURATION

The MA204 contains three sets of four switches that select the input threshold levels and impedance of the FPSIGA and FPSIGB front panel inputs, the mode of operation for the pulse generation logic, and the Sync Out level and impedance. The switches are located as shown in Figure 4. The switches are only accessible with the module removed from the carrier.

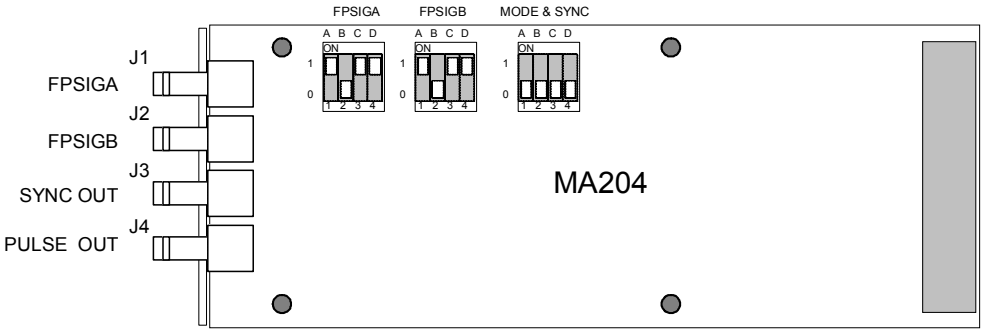

Figure 4. MA204 Hardware Configuration Switches

Front Panel Signals A & B Input Threshold Level These switches control the threshold level of the signal A and signal B front connector signals.

Signal Level	SIGA & SIGB Switches A	B
-2.0V	OFF	OFF
0V	OFF	ON
+1.2V	ON	OFF
+1.8V	ON	ON

Front Panel Signals A & B Input Impedance These switches select the input impedance of the signal A and signal B front connector signals.

Impedance	SIGA & SIGB Switches C	D
>100KΩ	OFF	OFF
180Ω	OFF	ON
82Ω	ON	OFF
56Ω	ON	ON

Mode These switches control special internal clock and fine delay modes of operation.

Switch A controls whether the internal period is generated using a variable or fixed frequency clock. The default for the -0001 version is OFF (variable clock), which provides a 100ps resolution when programming the pulse period. The -0001 version can use the fixed clock setting, if a pulse period resolution of only 5ns is required. The default for the -0002 version is ON (fixed clock), which provides a 5ns resolution. The -0002 version can use the variable clock mode, however, the pulse width resolution and pulse delay resolution will then vary from 5 to 10ns.

Internal Period Mode	Mode & Sync Switch A
Variable Clock (100ps res.)	OFF
Fixed Clock (5ns res.)	ON

Switch B controls whether the delay elements are used. The default for the -0001 version is OFF (fine delay enabled), which will provide 100ps pulse width and delay resolution. The fine delay can be disabled on the -0001 version; however, only 5ns resolution will then be provided. The -0002 version must always be set to ON (fine delay disabled) for proper operation.

Fine Delay Mode	Mode & Sync Switch B
Fine Delay Enabled (100ps res.)	OFF
Fine Delay Disabled (5ns res.)	ON

Sync Out Level & Impedance These switches control the output level and impedance of the Sync Out signal.

Sync Out Level (no load)	Mode & Sync Switch C
+5V	OFF
+9V	ON

Sync Out Impedance	Mode & Sync Switch D
50Ω	OFF
3Ω	ON

3.4 INPUT/OUTPUT SIGNALS

The front panel input/output signals are as shown in Figure 5 and are briefly described below. The connector shield of each of the connector is tied to chassis ground.

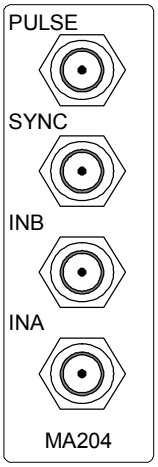

Figure 5. Front Panel

INA This SMA connector is the input signal A. This input is software configurable as the trigger, gate, or reference clock signal.

INB This SMA connector is the input signal B. This input is software configurable as the trigger, gate, or reference clock signal.

SYNC This SMA connector is the output Sync Out signal.

PULSE This SMA connector is the output pulse signal.

3.5 IDENTIFICATION AND CONFIGURATION REGISTERS

3.5.1 I/O Registers

There are a variety of registers used to configure and control the MA204 module. These registers are located in the IOSpace. The address map of the registers is shown in Table I. Details of the registers are provided in Figure 6.

Table I. I/O Address Map/Command Summary

MA204 IO REG. (HEX)	REGISTER DESCRIPTION
00	Control/Status
02	Interrupt Control
04	Trigger/Gate Control
06	Calibration
08	Pulse Period – Low
0A	Pulse Period – Mid
0C	Pulse Period – High (4 bits)
0E	Pulse Width – Low
10	Pulse Width – Mid
12	Pulse Width – High (4 bits)
14	Pulse Delay – Low
16	Pulse Delay – Mid
18	Pulse Delay – High (4 bits)
1A	Pulse Pair Delay – Low
1C	Pulse Pair Delay – Mid
1E	Pulse Pair Delay – High (4 bits)
20	Amplitude – Low
22	Amplitude – High
24	Slew Rate
26	Burst Count – Low
28	Burst Count – High

MA204
Reg. 00

Control/Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	SPO	SOE	RFE	-	REFSEL		-	POI	PPO	POE	PP	RMODE		RUN
Read	RDY	LOK	SPO	SOE	RFE	DET	REFSEL		-	POI	PPO	POE	PP	RMODE		RUN

RDY ⇨ Ready (1 = ready)
LOK ⇨ Oscillator Locked To Reference (0 = not locked, 1 = locked)
SPO ⇨ Sync Out Polarity (0 = normal (active high) (default), 1 = inverted (active low))
SOE ⇨ Sync Out Enable (0 = disabled (default), 1 = enabled)
RFE ⇨ Enable Reference Use (0 = disabled (default), 1 = enabled)
DET ⇨ Reference Detected (0 = not detected, 1 = detected)
REFSEL ⇨ Reference Clock Source Select (if enabled)
- 00 Front Panel Signal A
- 01 Front Panel Signal B
- 10 Backplane Trigger A
- 11 Backplane Trigger B

POI ⇨ Pulse Output Impedance (0 = low (default), 1 = 50Ω)
PPO ⇨ Pulse Polarity (0 = normal (active high) (default), 1 = inverted (active low))
POE ⇨ Pulse Output Enable (0 = disabled (default), 1 = enabled front panel output)
PP ⇨ Pulse Mode (0 = single pulse (default), 1 = pulse pair)
RMODE ⇨ Run Mode
- 00 Single pulse or pulse pair (default)
- 01 Continuously cycle
- 10 Burst count
- 11 Follow Trigger Input

RUN ⇨ Run (0 = enable (default), 1 = disable)

Notes:
1. Always set the RUN bit to 0 before changing the RMODE. Do not change the RMODE at the same time the RUN bit is changed (use separate write operations).
2. All unused bits should be written as 0's to ensure future revision compatibility.

MA204
Reg. 02

Interrupt Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	MIEN	-	-	-	-	-	-	IT	-	-	-	-	-	-	RIEN	BIEN
Read	MIEN	-	-	-	-	-	-	IT	-	-	RDI	EOB	-	-	RIEN	BIEN

MIEN ⇨ Master Interrupt Enable (0 = disabled (default), 1 = enable)
IT ⇨ Interrupt Type (0 = Type A, software-end-of-interrupt (default), 1 = Type C, hardware-end-of-interrupt)
RDI ⇨ Ready Interrupt (1 = Ready bit went high (write a 1 to this bit to clear))
EOB ⇨ End of Burst (1 = EOB occurred (write a 1 to this bit to clear))
RIEN ⇨ Ready Interrupt Enable (0 = disabled (default), 1 = enabled)
BIEN ⇨ End of Burst Interrupt Enable (0 = disabled (default), 1 = enabled)

Note: When using Type C interrupts (IT = 1), the interrupt pending bits 7-0 are presented as the interrupt vector during the interrupt acknowledge cycle. The interrupt is also disabled and must be re-enabled during the interrupt service routine.

Figure 6. MA204 I/O Registers

MA204
Reg. 04

Trigger/Gate Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SG	GM	-	-	GATESEL				MTRGSELB		MTRGSELA		TRGSEL			
Read	SG	GM	-	-	GATESEL				MTRGSELB		MTRGSELA		TRGSEL			

SG ⇨ Synchronous Gating (0 = asynchronous gating, 1 = synchronous gating)
GM ⇨ Gated Mode (0 = disabled, 1 = enabled)
GATESEL ⇨ Gate Source Select

	High Level		Low Level
0000	Ignore Gate (default)	1000	(reserved)
0001	Front Panel Signal A	1001	Front Panel Signal A
0010	Front Panel Signal B	1010	Front Panel Signal B
0011	(reserved)	1011	(reserved)
0100	Backplane M-Trigger A	1100	Backplane M-Trigger A
0101	Backplane M-Trigger B	1101	Backplane M-Trigger B
0110	(reserved)	1110	(reserved)
0111	(reserved)	1111	(reserved)

MTRGSELx ⇨ M-Trigger A and M-Trigger B Control

00	Trigger Input (default)
01	Output Pulse
10	Output Sync
11	Reserved

TRGSEL ⇨ Trigger Source Select

	Rising Edge		Falling Edge
0000	Software RUN bit (default)[1]	1000	(reserved)
0001	Front Panel Signal A	1001	Front Panel Signal A
0010	Front Panel Signal B	1010	Front Panel Signal B
0011	(reserved)	1011	(reserved)
0100	Backplane M-Trigger A	1100	Backplane M-Trigger A
0101	Backplane M-Trigger B	1101	Backplane M-Trigger B
0110	(reserved)	1110	(reserved)
0111	(reserved)	1111	(reserved)

Notes:
1. Setting the RUN bit will cause a pulse or pulse train to occur.
2. All unused bits should be written as 0's to ensure future revision compatibility.

MA204
Reg. 06

Calibration

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	CRST	-	-	-	CALVAL											
Read	CRST	-	-	-	CALVAL											

CRST ⇨ Calibration Reset (0 = Calibration Enabled, 1 = Reset Calibration)
CALVAL ⇨ Calibration Value (see 4.2 for details)

Notes:
1. CRST must be set to zero in order to set CALVAL.
2. Writing a one to CRST will set CALVAL to its default value of 0xFFF.

Figure 6. MA204 I/O Registers (continued)

MA204 Reg. 08

Pulse Period - Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA204 Reg.0A

Pulse Period - Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							Middle Order Bits								16
Read	31							Middle Order Bits								16

MA204 Reg.0C

Pulse Period - High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													35	High Bits		32
Read													35	High Bits		32

Note: Each bit represents 100ps. The registers must be written in the order low, mid., and then high. The new pulse period does not take effect until the high order register is written.

MA204 Reg. 0E

Pulse Width - Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA204 Reg. 10

Pulse Width - Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							Middle Order Bits								16
Read	31							Middle Order Bits								16

MA204 Reg. 12

Pulse Width - High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													35	High Bits		32
Read													35	High Bits		32

Note: Each bit represents 100ps. The registers must be written in the order low, mid., and then high. The new pulse width does not take effect until the high order register is written.

Figure 6. MA204 I/O Registers (continued)

MA204 Reg. 14

Pulse Delay - Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA204 Reg. 16

Pulse Delay - Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							Middle Order Bits								16
Read	31							Middle Order Bits								16

MA204 Reg. 18

Pulse Delay - High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													35	High Bits		32
Read													35	High Bits		32

Notes:

1. Each bit represents 100ps with 0 equal to the minimum delay (see note 3).
2. The registers must be written in the order low, mid., and then high. The new pulse delay does not take effect until the high order register is written.
3. The time to an un-delayed output pulse as specified in Section 1.2.2, Sync Out Characteristics, must be taken into account when programming the desired pulse delay time.

MA204 Reg.1A

Pulse Pair Delay – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA204 Reg.1C

Pulse Pair Delay – Mid

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							Middle Order Bits								16
Read	31							Middle Order Bits								16

MA204 Reg. 1E

Pulse Pair Delay – High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write													35	High Bits		32
Read													35	High Bits		32

Notes:

1. Each bit represents 100ps with 0 equal to 0ns.
2. The registers must be written in the order low, mid., and then high. The new pulse delay does not take effect until the high order register is written.

Figure 6. MA204 I/O Registers (continued)

MA204
Reg. 20

Output Amplitude - Low Level

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	See Note											
Read	-	-	-	-	See Note											

Note: Each bit represents 2.2mV with zero representing -2.0V.

MA204
Reg. 22

Output Amplitude - High Level

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	See Note											
Read	-	-	-	-	See Note											

Note: Each bit represents 2.2mV with zero representing -2.0V.

MA204
Reg. 24

Slew Rate

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	See Note											
Read	-	-	-	-	See Note											

Note: Each bit represents 366 mV/µs with zero representing 1000V/us.

MA204
Reg.26

Burst Count – Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	15							Low Order Bits								0
Read	15							Low Order Bits								0

MA204
Reg.28

Burst Count - High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	31							High Order Bits								16
Read	31							High Order Bits								16

Note: The registers must be written in the order low then high. The new burst count does not take effect until the high order register is written.

Figure 6. MA204 I/O Registers (continued)

3.5.2 M-Module Identification PROM

The MA204 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.5.

The modules also support the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

Table II. M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00CC (204 dec.)
2	Revision Number[1]	0002
3	Module Characteristics[2]	1E68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[3]	FFE7 (MA204)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the functional revision level of the module. It does not necessarily correspond to the hardware assembly level.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	1 = trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE7_{16}$ = C&H specified VXI model code for MA204

4.0 OPERATION

The MA204 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.5.1. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

4.1 PROGRAMMING

4.1.1 Writing Register Values

Normal 16-bit wide register values can be written in one write operation using 16-bit register access. However, some pulse parameters, such as the pulse period, pulse width, and pulse delay, require more than 16-bits. Special attention must be given when programming these values. To prevent a pulse parameter from changing until the entire value is written, the order of the write operations is important. The internal logic is configured to only accept the change when the high-order bits are written. Therefore, the application software must write the low bits first, then the middle bits, and lastly the high bits.

4.1.2 Pulse Programming

With the RUN bit disabled (0) in the Control/Status register, set the desired pulse period, pulse width, pulse delays, high/low amplitude, desired trigger control mode, pulse mode (single or pulse pair), and run mode (single, continuous, or burst pulse). After setting the desired pulse parameters, a finite amount of time (<50ms) is required for configuration of the internal logic. The module will signal that it is ready to run by setting the RDY bit. Application software should verify the module is ready by reading the RDY bit. If desired, an interrupt can be generated to signal this event. Once the RDY bit is verified, enable the RUN bit (1). Modifications can be made to all settings except for RMODE without clearing the RUN bit; however, the RDY bit will go low momentarily and there may be a pulse glitch while the configuration is being adjusted.

4.1.2.1 Pulse Delay

The pulse delay is defined as the amount of time from the leading edge of Sync Out to the leading edge of the output pulse. Pulse delay is user programmable from 0 to 5.2 seconds in 100ps steps. When programming the pulse delay, the intrinsic delay specified in Section 1.2.2, Sync Out Characteristics, "Time to un-delayed output pulse", must be considered. The actual delay from Sync Out to Pulse Out is equal to the intrinsic delay plus the programmed pulse delay.

When programming the Pulse Pair Delay, the above mentioned intrinsic delay does not have to be taken into account. See 4.1.3 for further details.

4.1.2.2 Sync Out

Sync Out will always precede an un-delayed output pulse by the amount of time specified in Section 1.2.2, Sync Out Characteristics, Time to un-delayed output pulse. This time must be taken into account when programming the desired pulse delay time.

In addition, when using external triggering, it is important to keep in mind the maximum time from external trigger to Sync Out time as specified in Section 1.2.2, Sync Out Characteristics. This time is due to intrinsic logic delays and the required synchronization of the asynchronous external trigger to the internal clock on the MA204. Because the input trigger and internal clock are independent of one another, the time from the external trigger to Sync Out will jitter 5-10ns from trigger to trigger.

Sync Out's pulse width has three different ranges and can vary within a range depending on the programmed period. As the variable clock's period changes between 20-40ns (see 4.1.2.3), the Sync Out's pulse width is directly affected. For pulse periods smaller than 80ns, the pulse width is half that of the variable clock. For pulse periods >80ns and <5µs Sync Out's pulse width is twice that of the variable clock, and for periods ≥ 5µs sync out's pulse width is equal to 40ns.

4.1.2.3 Period Programming Resolution

The programmed period is derived from a variable clock feeding into a 30-bit counter. For period's ≥5µs, the clock speed is set at 20ns and for periods <5µs the clock varies from 20 to 40ns in 20ps increments to increase period resolution. The variable clock frequency is then multiplied by 4 to run the counters at a higher resolution (i.e. a 20ns clock period drives the counter at 5ns of resolution).

The counters were designed to count in multiples of two. For example, to get a 240ns period, the variable clock is set for 30ns, which is then frequency multiplied by 4 to run the counters at 7.5ns, and the counters are set to count to 32. To get a period of 120ns, the same clock runs a counter to 16. However, as the multiple of two increases, the overall period resolution decreases. 20ps x 4 = 80ps, x8 = 160ps, x16 = 320ps; until 5µs is reached as which point the resolutions is greater than 5ns. For periods greater than 5µs, the variable clock is set at 20ns and the counters increment accordingly for the desired period, abandoning the two's multiple approaches.

To complicate matters, the nature of the variable clock does not allow it to make every 20ps step between periods of 20-40ns. The unachievable frequencies are: 20.02ns, 26.66ns, 29.98ns, 30.02ns, 33.34ns, 36.66ns, 37.14ns, and 39.98ns.

These six frequencies represent gaps in programmable frequencies when the counter multiple is greater than 5x or beginning at 160ns. Therefore, the specification shows the worst case resolution for a period of 80-160ns equal to 160ps, because of these six gaps. At all other frequencies in this range, the resolution is actually 80ps. From 160-320ns, the gaps cause a resolution of 320ps while there is a resolution of 160ps over the majority of the range.

4.1.2.4 Minimum Pulse Period

For periods between 20 and 40ns the counters are bypassed, and the variable clock drives the Pulse Out and Sync Out signals directly. In effect, for periods within this range, the duty cycle is set to 50%, Pulse Pair is disabled, and the actual pulse delay becomes essentially 0ns. All other operations are still possible, i.e. single pulse, burst count, triggering, and gating.

4.1.3 Single Pulse vs. Pulse Pair

The PP bit in the Control/Status Register selects whether a single pulse (or pulse pair) occurs when the pulse is triggered. It is important to remember that the Pulse Pair Delay is the time from the rising edge of the first pulse to the rising edge of the second pulse; therefore, the Pulse Pair Delay should be set to a value greater than the Pulse Width. If a value less than that amount is set, the MA204 will automatically begin the second pulse immediately after the falling edge of the first pulse.

4.1.4 Single, Continuous, and Burst Modes

The RMODE bits in the Control/Status Register selects whether a single pulse (or pulse pair) or a series of pulses is output for each software run or external trigger. To output a continuous stream of pulses, set the RMODE to Continuous Cycle mode, then the RUN bit to 1. If the Trigger Source in the Trigger/Gate Control register is set to "Software RUN bit," the pulses will start immediately. Otherwise, the pulse will start when the selected trigger becomes active. To stop the stream of pulses, set the RUN bit to 0. To output a specific number of pulses, set the Burst Count registers to the desired number, then set the RMODE to Burst mode. Use the software RUN bit or an external trigger to initiate the output of the desired number of pulses. The burst of pulses are output each time the RUN bit or external trigger go from inactive (0) to active (1). If desired, an interrupt can be generated at the end of the burst (see 4.4 for details).

> **NOTE: Always set the RUN bit to 0 before changing the RMODE. Do not change the RMODE at the same time the RUN bit is changed (use separate write operations).**

4.1.5 Follow Trigger Mode

Setting the RMODE bits in the Control/Status Register to "Follow Trigger Input" causes the output pulse to follow both the pulse width and period of the selected Trigger Source specified in the Trigger/Gate Control register. This feature can be used to provide level shifting of an input signal.

4.1.6 Pulse Gating

Pulse output can be enabled only during the presence of an external signal by setting the Gate Mode (GM) bit to a 1 in the Trigger/Gate Control register. Select the gate source using the GATESEL bits and select either synchronous or asynchronous gating with the SG bit. With synchronous gating, the first pulse is synchronized with the rising edge of the gate signal. With asynchronous gating, the pulses internal free run and the output is disabled when the gate signal is inactive.

4.2 CALIBRATION

Calibration is <u>not</u> required for normal operation. It is only used to improve the stated accuracy for pulse width, pulse delay and pulse pair delay on -0001 versions of the MA204. To improve these accuracies, a calibration register is provided that allows minor adjustments to be made to compensate for temperature and process variation of the fine delay elements. The register is not used on -0002 versions. Without calibration, the programming steps may be slightly longer or shorter on average than 100ps.

To adjust the calibration value, first, reset the calibration register to $0FFF_{16}$. Then set the period registers to a value of $0000031FF_{16}$, and the pulse width to $0000001F4_{16}$. Enable a continuous pulse out with 50Ω output impedance by writing a 0052 to the control register. Set an appropriate output amplitude level and write $0FFF_{16}$ to the slew rate register. Begin pulsing by writing 0053_{16} to the control register. Next, use a calibrated instrument to measure the output pulse width; it should be around 50ns. Finally decrease the pulse width 100ps by writing $0000001F3_{16}$ to the pulse width register.

With CALVAL set to $0FFF_{16}$, the pulse width should have increased rather then decrease by 100ps. Add the amount the pulse width increased to 9.9ns, and then divide this value into 9.9ns to get a ratio. Multiply this ratio by $0FFF_{16}$ (4095) to determine the new CALVAL. Set CALVAL to its new value and repeat the test. The pulse width should decrease by exactly 100ps. Minor adjustments to CALVAL may be necessary to adjust pulse width within desired accuracy.

4.3 REFERENCE DISCIPLINING

The MA204's internal oscillator can be disciplined to an external clock, by selecting the reference clock source (REFSEL bits) in the control/status register. If a 10MHz reference clock is detected, the DET bit in the control/status will be a one. Enable disciplining by writing a one the RFE bit in the control/status register. When the internal clock is disciplined to within approximately one decade of the reference clock, the LOK bit will transition high. The MA204 will continue to discipline itself to the reference clock as long as the reference clock is present.

Once locked status is achieved, the reference may be disabled and removed. The MA204 will hold its internal clock at the locked frequency, although some drift will eventually occur. If the reference is removed, the RFE bit will automatically be set to a zero and will need to be rewritten high once the reference is again detected.

4.4 INTERRUPTS

The MA204 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Interrupt Control Register to configure the desired type of interrupt.

For an interrupt to occur, the desired interrupt source must be enabled (RIEN or BIEN) and the master interrupt enable (MIEN) must be enabled in the Interrupt Control Register. For Type C interrupts, the interrupt vector is equal to the lower byte of the interrupt control register.

> NOTE: For any interrupt to occur, the MIEN bit in the Interrupt Control Register must be set to a one.

End of Burst The End of Burst bit (EOB bit) is set to a one when the burst of pulses is complete. It remains a one until a 1 is written to the bit to clear it. Enable an interrupt on this condition by writing a one to the BIEN and MIEN bit in the Interrupt Control Register.

Ready The Ready Interrupt (RDI bit) is set to a one when the module becomes ready for operation following a change in the pulse period, width, delay, or other operational mode. It remains a one until a 1 is written to the bit to clear it. Enable an interrupt on this condition by writing a one to the RIEN and MIEN bit in the Interrupt Control Register.

> NOTE: When using Type C interrupts, the MIEN bit is cleared during the interrupt acknowledge cycle. It must be re-enabled to receive another interrupt.

4.5 ID PROM

Refer to 3.5.2 for a description of the ID PROM's function and contents. The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. Figure 7 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_eebyte (addr, id_addr);
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_eebit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_eebit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_eebit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 7. ID PROM Access Routine

APPENDIX A: CONNECTORS

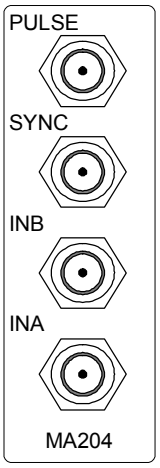

Figure A-1. Front Panel I/O Signals

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
A14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

Figure A-1. M/MA Interface Connector Configuration

N O T E S:

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