U S E R ' S M A N U A L

16-CHANNEL
EVENT DETECTOR

MODEL
MA203

Document Part No: 11028104C

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NOTE

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INTRODUCTION

This manual describes the operation and use of the C&H Model MA203 MA-Module (Part Number 11028100) and the associated AM104 Input Signal Conditioning modules (Part Number 11028120). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. A software driver using high level function calls may be available, please contact C&H for information.

The part numbers covered by this manual are:

Part Number	Description
11028100-0001	MA203 Event Detection MA-Module
11028120-0001	AM104 +5V Optocoupled Input
11028120-0002	AM104 +28V Optocoupled Input
11028120-0003	AM104 Contact Closure Sensing
11028120-0004	AM104 Programmable Threshold

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1. GENERAL DESCRIPTION

The MA203 is a 16-channel event detection module with selectable input types provided through a plug-in daughter card signal conditioning accessory modules. Signal conditioning AM104 accessory modules are used to individually provide programmable threshold, optocoupled +5V input, +28V input, and contact closure sensing. Other input types may also be available.

The module selectively stores and buffers up to 32K time-value pairs in a FIFO. Since a time-value pair is only stored when selected inputs change, considerable data compression is possible for slow changing inputs, while still maintaining change sequence timing during very active times. Extensive interrupt support allows user software to be interrupted when data is stored, the FIFO is half-full, the FIFO is full, on the change-of-state or level transition of any input, or on a specific bit pattern.

The module is physically implemented on a single wide MA-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The MA203 may be installed in any carrier board supporting the M-Module specification.

1.1. PURPOSE OF EQUIPMENT

This MA-Module is especially well suited for data acquisition of digital signals, including contact closures. The module can be used to monitor data inputs and record their transition times. Interrupts can be generated on data changes or on the presence of a specific bit pattern. The 32K FIFO allows time-related data retrieval of fast transient type digital signals.

1.2. SPECIFICATIONS OF EQUIPMENT

1.2.1. Features

- Number of Input Channels: 16
- Sample Rate: 5MHz (maximum)*
- Input Debounce: 0 to 128ms, software selectable
- Input Polarity: Software selectable
- Input Type: Plug-in accessory module defines input specifications
- Interrupts: Data stored, FIFO half-full, FIFO full, time-stamp rollover, any input change-of-state or level transition, bit pattern
- Local Memory: 32K time-value data pairs (31-bit time-stamp, 16-bit data)
- Data Retrieval: FIFO data port register allows rapid data retrieval
- Sampling Strobe: Internal, External Front Panel signal or Backplane Trigger (source and prescaler are software programmable)
- On-Board Power Supply: On-board isolated power supply for contact closure sensing

* The type of input conditioning module may limit signal frequency. See specifications for each individual accessory module for details.

1.2.2. Base Module Specifications

For input specifications, refer to Section 1.2.3.

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V (base module only)	400	mA
	+12V (base module only)	0	mA
	-12V (base module only)	20	mA
+12VSUP & -12VSUP Supply Current		100	mA max.
ISOVPOS Supply Current	when using contact accessory module	50	mA max.
	when using other accessory module	100	mA max.
Maximum Voltage on External Inputs	50Ω input impedance	5	Vrms max.
	>100KΩ input impedance	16	Vrms max.

SPECIFICATIONS (full operating temperature, unless otherwise specified)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Internal Sample Clock					
Accuracy				±100	ppm
Frequency	Input modules may limit (see note)			5 [1,2]	MHz
Jitter				±500	ps
External Inputs (EXTCLK/EXTRUN)					
Input Threshold	Switch selectable	-0.2	0	+0.2	V
		+0.6	+0.8	+1.0	V
		+2.3	+2.5	+2.7	V
Impedance	Switch selectable	48	50	52	Ω
		100K			Ω
Frequency	EXTCLK			5	MHz
	EXTRUN			1	MHz
Isolated Supply					
Output	10% load		5.7		V
	100% load		4.7		V
Isolation		1000			Vrms

Notes:
1. Input conditioning modules may limit the sample frequency. Refer to Section 1.2.3 for details.
2. The internal clock rate is software selectable to 10KHz, 100KHz, 500KHz, or 5MHz. A prescaler allows further control.

1.2.3. Accessory Module Specifications

The following AM104 accessory modules are currently available. Other input types are possible and may already be available. Please check with C&H for details. These modules are individually described in the appendices of this document starting with Appendix B.

Part Number	Description	Appendix
11028120-0001	AM104 +5V Optocoupled Input	B
11028120-0002	AM104 +28V Optocoupled Input	C
11028120-0003	AM104 Contact Closure Sensing	D
11028120-0004	AM104 Programmable Threshold	E

1.2.4. Electrical

The MA203 requires the +5V and ±12V power from the M-Module carrier.

1.2.5. Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082"(52.9 mm) wide.

1.2.6. Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

Carrier modules may differ in environmental specification. Refer to the carrier's documentation for information.

1.2.7. Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	MA-Module
Addressing:	A08
Data:	D16
Interrupts:	INTA & INTC
DMA:	not supported
Triggers:	Input/Output Trig A and Trig B
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$ (VXI-IDENT Code)
Device Type:	$FFE8_{16}$ (VXI-IDENT Code)
Model Number:	$00CB_{16}$ (M-Module IDENT Code)

1.2.8. Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2. INSTALLATION

2.1. UNPACKING AND INSPECTION

In most cases the MA203 is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2. HANDLING PRECAUTIONS

The MA203 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3. INSTALLATION OF M-MODULES

> CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

All M-Modules must be installed into the carrier before the carrier is installed into the host system. M-Modules are installed by firmly pressing the connector on the M-Module together with the connector on the carrier. Secure the M-Module with mounting hardware provided as shown in Figure 1.

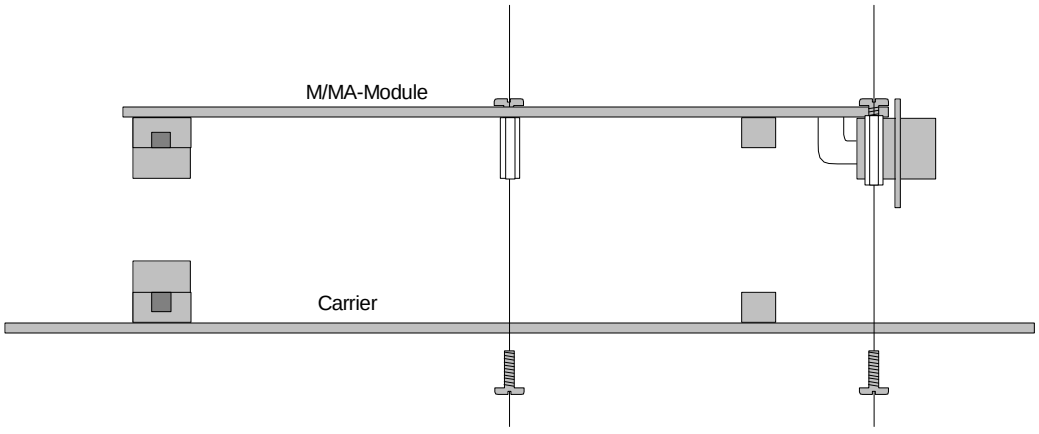


Figure 1. M-MODULE Installation

2.4. PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module-shipping container and packing material may be re-used if it is still in good condition.

3. FUNCTIONAL DESCRIPTION

3.1. GENERAL

The MA203 provides 16-channel digital input and selective storage at a rate up to 5 million samples per second (MSPS). Input signals are translated and conditioned through a plug-in daughter card accessory module. The conditioned signals are debounced then sampled at the configured clock rate. If any of the desired inputs changed state from the last stored value, the new data and the current time-stamp are stored in the FIFO.

The base MA-Module contains all common electronics to debounce the conditioned signals from the accessory module, alter active polarity, selectively store and time-stamp the data value, and provide interrupts on change-of-state, level transition, or a bit pattern. An isolated DC-DC converter is provided for contact sensing operation.

Data is stored along with a 31-bit time stamp allowing almost 6 hours of uniquely time stamped data to be monitored at a resolution of 10µs. The time-value pairs of data are stored in memory and retrieved by the user in a first-in first-out (FIFO) manner. Data is read through a single FIFO data port register allowing rapid data retrieval. The most significant bit of the upper time-stamp field indicates data validity (or FIFO empty). A simplified block diagram of the module is shown in Figure 2. Input channel logic flow shown is shown in Figure 3.

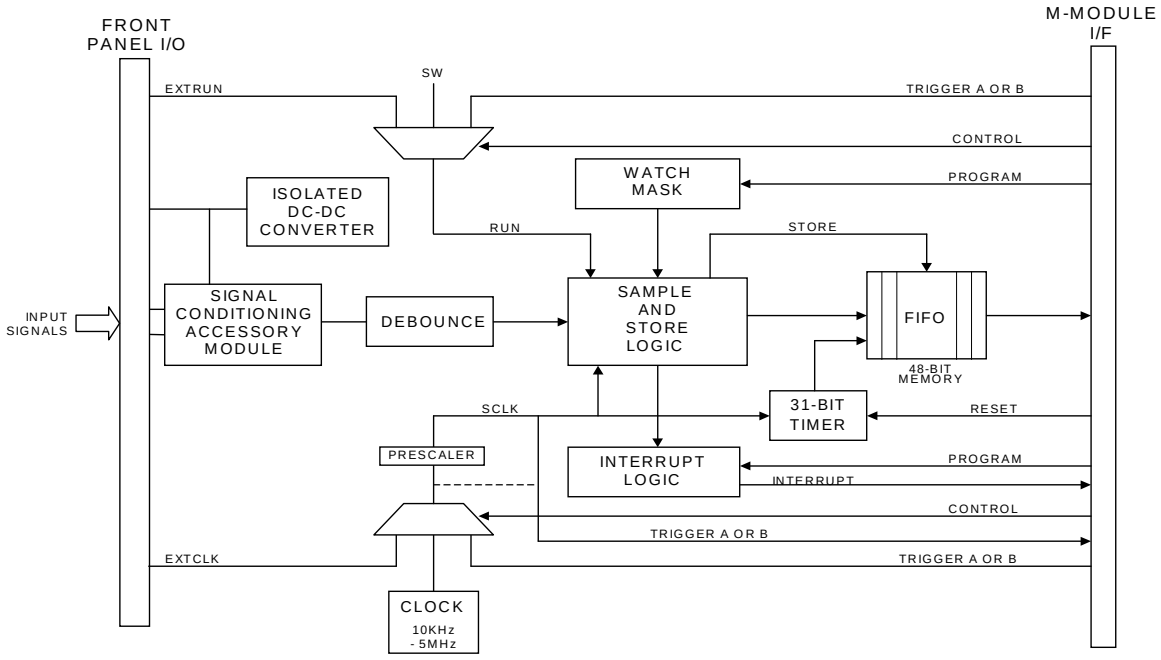


Figure 2. Functional Block Diagram

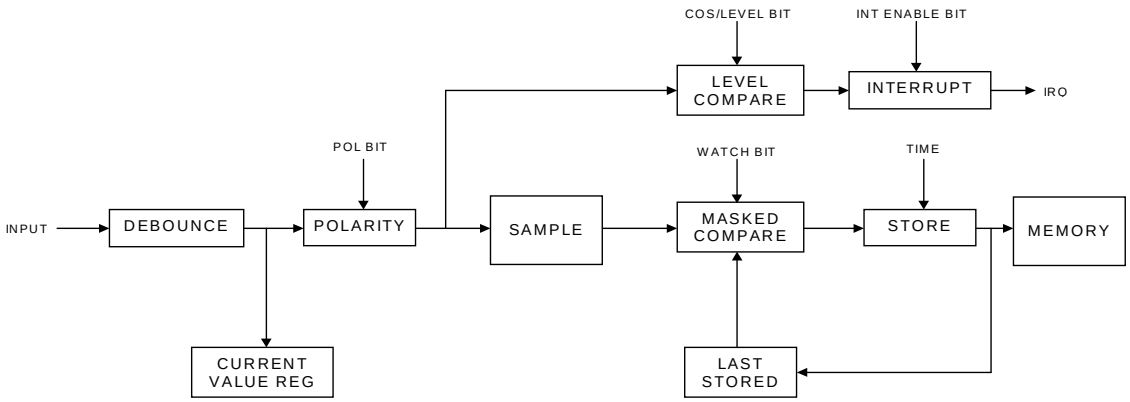


Figure 3. Input Channel Logic Flow

3.1.1. Isolated DC-DC Converter

The DC-DC Converter provides an isolated (1000Vrms) 5V unregulated supply to the signal conditioning accessory module for contact closure sensing. Unregulated voltage varies from 5.7V at 10% load to 4.7V at 100% load.

3.1.2. Debounce

The debounce logic provides individual signal debounce to eliminate contact bounce and transient noise glitches. The debounce time is software selectable from 0 to 128ms. Each group of four inputs (0-3, 4-7, 8-11, and 12-15) may have a different debounce time.

3.1.3. Sample and Store Logic

The sample and store logic samples the debounced and polarity conditioned signal and then compares the new data value with the last stored value. If the new value is different, then the new data value is stored in the FIFO memory along with the 31-bit timer value (time-value pair). The first time-value pair captured after the sampling is enabled is automatically stored, since a last stored value may not exist. The last time-value pair captured after the sampling is disabled, is also automatically stored to give an end point reference time and value.

3.1.4. Watch Mask

The watch mask allows any bit(s) or group of bits to be ignored, so that only changes in the desired bits cause storage of the data and timestamp. The watch mask only affects the storage of the data. It does not affect the interrupt logic.

3.1.5. Interrupt Logic

The interrupt logic monitors the sampled data for change-of-state, level transition, or a bit pattern depending on the interrupt definition. If a change-of-state, level transition, or a specified bit pattern occurs an interrupt pending latch is set and an interrupt request is applied. A pending interrupt can only be cleared by writing a 1 to the individual bit in the Interrupt Pending/Clear Register. If additional interrupts occur during interrupt latency or processing, the interrupt is latched. The interrupt request remains applied until all latched interrupts are cleared.

3.1.6. 31-Bit Timer

This 31-bit timer provides a time stamp of the data stored. The timer increments by one for each rising edge of the sample clock. Almost 6 hours of uniquely time-stamped data can be captured when running a sample rate of 100K samples per second.

3.1.7. FIFO

The synchronous read/write first-in first-out (FIFO) memory provides data storage for up to 32K time-value pairs. The time-value pairs are stored as 48-bit wide data and retrieved by the user as a three 16-bit words.

3.1.8. Clock

The clock logic allows selection of the internal time base, front panel input clock, or backplane trigger signal as the sample clock. The logic also allows selection of either 10KHz , 100KHz, 500KHz, or 5MHz as the internal time base. A prescaler of 1, 2, 5, 10, 20, 50, 100, or 200 can also be applied to the chosen sample clock source.

3.1.9. Signal Conditioning Accessory Module

The signal conditioning accessory module provides input signal translation and/or isolation.

3.2. HARDWARE CONFIGURATION

Switch selectable options are shown in Figure 4.

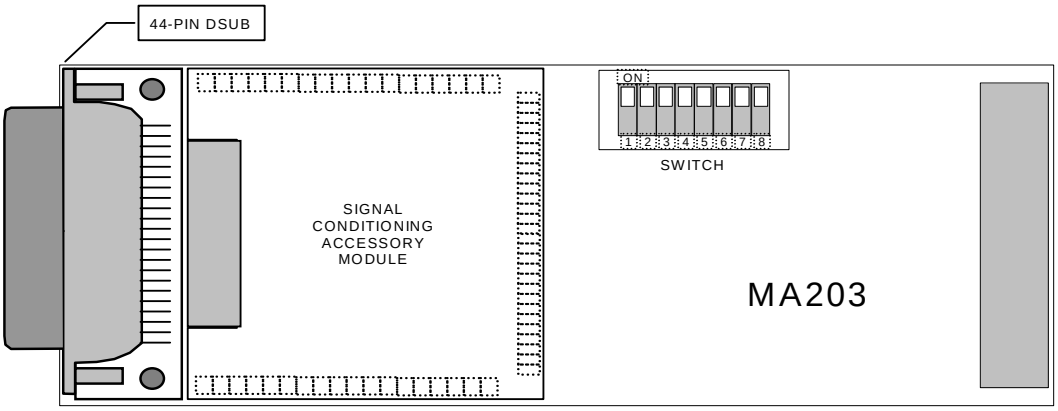


Figure 4. Hardware Configurable Controls

EXTCLK/EXTRUN Impedance (Z) These switches select the input impedance of the EXTCLK and EXTRUN front connector signals.

Impedance	EXTCLK SW1	EXTRUN SW5
50Ω	ON	ON
>100KΩ	OFF	OFF

EXTCLK/EXTRUN Level These switches control the threshold level of the EXTCLK and EXTRUN front connector signals. The level can be set to 0V (zero crossing), TTL (0.8V), or CMOS (2.5V).

	EXTCLK		EXTRUN	
Signal Level	SW2	SW3	SW6	SW7
0V	OFF	OFF	OFF	OFF
TTL	ON	ON	ON	ON
CMOS	ON	OFF	ON	OFF

3.3. CONNECTORS

3.3.1. M/MA Interface Connector

The M.MA-Module interface connector contains signal and voltage connections specific to the M-Module interface. (See Appendix A for pin assignments)

3.3.2. Front Panel I/O Connector

The front panel I/O connector is a standard 44-pin D-subminiature female receptacle. Below are the signals and functional descriptions provided on the connector. (See Appendix A for pin assignments)

INA0(+) to IN15(+)	Digital Inputs 0 - 15 (POS) *(Input, level and signal type depends on accessory module option installed)*
INB0(-) to INB15(-)	Digital Inputs 0 - 15 (RTN) *(Input, level and signal type depends on accessory module option installed)*
EXTCLK	External Clock. This signal can be used for timing the data sampling. *(Input, 5MHz max., level and impedance is switch selectable, see 3.2)*
EXTRUN	External Run. This signal can be used to enable/disable sampling and data storage. *(Input, level and impedance is switch selectable, see 3.2).*
GND (LOGIC)	Digital Logic Ground *(common ground for EXTCLK, EXTRUN, +12VSUP, -12VSUP)*
ISOVPOS	Positive side of 5V unregulated isolated power supply. Used by the contact closure signal conditioning accessory module, but can also be used externally. *(Do not exceed 50mA when using contact closure accessory module, otherwise do not exceed 100mA)*
ISOVNEG	Negative side (Return) of 5V unregulated isolated power supply.
+12VSUP	+12V supply. Can be used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*
-12VSUP	-12V supply. Can be used for external buffer, amplifier, or other logic. *(Do not exceed 100mA)*

3.3.3. M-Module Peripheral Connector

The M-Module peripheral connector allows connection of certain signals to carrier boards that support this option. In accordance with the M-Module specification, the peripheral connector only has 24 pins available, and therefore, can not support all of the signals provided at the front panel connector. (See Appendix A for pin assignments)

3.3.4. Accessory Module Connectors

These connectors provide the signal interface between the MA203 base module and the signal conditioning accessory modules. (See Appendix A for pin assignments)

3.4. INDENTIFICATION AND CONFIGURATION REGISTERS

3.4.1. M-Module Identification

The MA203 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in I/O space and the data is read one bit at a time.

The MA203 also supports the VXI-IDENT function introduced by Hewlett-Packard. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table I.

Table I. M/MA Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00CB (203 dec.)
2	Revision Number	0001
3	Module Characteristics[1]	1A68
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type[2]	FFE8
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	1 = needs ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	1 = trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type C (type A also supported)
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

2) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FE8_{16}$ = C&H specified model code

3.4.2. IO Registers

There are a variety of registers used to configure and control the MA203 module. The registers are addressable within the I/O Space. An address map of the registers is shown Table II. The registers provide general control, status, sampling rate and source selection, interrupt enabling and transition control, clearing of the time stamp and memory, and reading of the captured time-value pairs. Details of the registers are provided in Figure 5.

Table II. I/O Address Map

IO Address, hex	Register Description
00	Control/Status
02	Clock Control
04	Master Interrupt Control
06	Debounce Control
08	Polarity
0A	Watch
0C	Channel Interrupt Enable
0E	Interrupt Definition
10	Interrupt Pending/Clear
12	FIFO Data Port
14	Current Value
16	Last Value Stored
18	FIFO Unread Count
1A	Accessory Module Control

Control/Status Register (00_{16}) This read/write register provides the main control of the module operation. Bits are provided for control of the run signal sources, reset of the FIFO and time stamp, manual conversion, and status of FIFO data storage.

Clock Control Register (02_{16}) This read/write register provides the control of the sampling clock. Bits are provided for control of the sampling clock source, prescaler, internal clock rate, and output trigger operation.

Master Interrupt Control Register (04_{16}) This read/write register enables interrupts and defines the interrupt vector value returned by the M-Module during an interrupt acknowledge cycle.

Debounce Control (06_{16}) This read/write register controls the debounce time of each group of four inputs.

Polarity (08_{16}) This read/write register inverts the active level of selected inputs before processing of interrupt or storage logic.

Watch ($0A_{16}$) This read/write register selects the input channels to watch when making the storage decision. The watch mask does not affect the interrupt logic. In other words, an ignored input may still cause an interrupt.

Channel Interrupt Enable ($0C_{16}$) This read/write register individually enables an input channel to be a source of an interrupt.

Interrupt Definition ($0E_{16}$) This read/write register allows definition of when an interrupt is to occur. If the Pattern (PAT) bit in the Master Interrupt Control Register is 0, then the Interrupt Definition Register selects interrupting on any change-of-state (low-to-high or high-to-low transition) or a change to the active level (inactive-to-active). The Channel Polarity Register selects the active level. If PAT = 1, then the Interrupt Definition Register specifies the a bit pattern that is required before an interrupt occurs. In this case, the Channel Interrupt Enable Register specifies "Don't Care" bits.

Interrupt Pending/Clear (10_{16}) This read/write register provides the interrupt status of each channel and clears a pending on write. The interrupt request will remain active until all pending interrupts are cleared by writing a one to the appropriate bit.

FIFO Data Port Register (12_{16}) This read-only register allows fast retrieval of stored time-value data pairs. Three 16-bit words are read in sequential order. The most significant bit (MSB) of the first word (the DV bit) determines which word is returned on the next read. If the MSB is 1, word 2 is returned followed by word 3 on the next read. If the MSB is 0, then word 1 continues to be returned. This allows the FIFO to continuously read until the DV bit goes low. Following a reset of the FIFO, word 1 is always the first word read from the FIFO Data Port.

Last A/D Value Stored Register (14_{16}) This read-only register provides the value of the last A/D value stored in memory. This register is typically only used for diagnostics purposes.

Current Value Register (16_{16}) This read-only register provides the current state of the inputs after the debounce logic.

FIFO Unread Count Register (18_{16}) This read-only register provides a count of the number of time-value pairs that have not been read from the FIFO port. This register is typically only used for diagnostics purposes.

Accessory Module Control Register ($1A_{16}$) This read/write register is used to identify and possibly control an AM104 accessory module.

Control/Status Register

00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DS	FF	HF	TSR	DC	-	-	-	STA	RUNSEL			SMP	RFF	RTS	RUN
Read	DS	FF	HF	TSR	DC	-	-	-	STA	RUNSEL			0	0	0	RUN

DS ⇨ Data Stored (1 = at least one time-value pair remains stored in the FIFO) [1]
FF ⇨ FIFO full (1 = FIFO is full, time-value pair storage stopped when the FIFO is full) [2]
HF ⇨ FIFO half-full (1 = FIFO is half-full) [1]
TSR ⇨ Time Stamp Rollover (1 = time stamp rollover occurred) [3]
DC ⇨ Debounce Control (0 = 0-128ms (slow), 1 = 0-3.28ms (fast))
STA ⇨ Store all (1 = ignore watch settings and store all values read)
RUNSEL ⇨ Run Source Select (always set to 000 before changing to any other value)

000	Software Run bit	100	Backplane Trigger A (high level)
001	(reserved)	101	Backplane Trigger A (low level)
010	EXTRUN FP signal (high level)	110	Backplane Trigger B (high level)
011	EXTRUN FP signal (low level)	111	Backplane Trigger B (low level)

SMP ⇨ Sample (a write of a 1 causes a single sample clock to occur)
RFF ⇨ Reset FIFO (1 = reset) [4]
RTS ⇨ Reset Time Stamp Clock (1 = reset) [4]
RUN ⇨ Run (if RUNSEL = 000, then 1 = enable sampling and storage)

Notes:
1) DS and HF indicate the current status of the FIFO.
2) FF is considered an error condition and can only be reset with a reset FIFO (RFF) or card reset.
3) TSR is cleared by writing a 1 to the bit.
4) The FIFO and Time Stamp Clock should only be reset when stopped (RUN and RUNSEL = 0).
5) A 1 must be written to the DS, FF, HF, and TSR bits to clear a pending interrupt.

Clock Control Register

02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	COS	TO	TS	-	-	ICLK		-	PSC			-	CLKSEL		
Read	-	COS	TO	TS	-	-	ICLK		-	PSC			-	CLKSEL		

COS ⇨ Clock Out Select (0 = internal clock before prescaler, 1 = sample clock, which is after prescaler)
TO ⇨ Clock Out to Trigger Out (1 = enable)
TS ⇨ Trigger Out Select (0 = Trigger A, 1 = Trigger B)
ICLK ⇨ Internal Clock Rate

00	10KHz	10	500KHz
01	100KHz	11	5MHz

PSC ⇨ Prescaler Control (Selected clock is divided by this prescaler)

000	Prescaler = 1	100	Prescaler = 20
001	Prescaler = 2	101	Prescaler = 50
010	Prescaler = 5	110	Prescaler = 100
011	Prescaler = 10	111	Prescaler = 200

CLKSEL ⇨ Clock Select

000	Internal Clock	100	Backplane Trigger A (rising edge)
001	(reserved)	101	Backplane Trigger A (falling edge)
010	EXTCLK FP signal (rising edge)	110	Backplane Trigger B (rising edge)
011	EXTCLK FP signal (falling edge)	111	Backplane Trigger B (falling edge)

Figure 5. I/O Registers

Master Interrupt Control Register

04

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	DIEN	FIEN	HIEN	TIEN	-	IT	IE	PAT	Interrupt Vector							
Read	DIEN	FIEN	HIEN	TIEN	-	IT	IE	PAT	Interrupt Vector							

DIEN ⇨ Enable interrupts on data stored
FIEN ⇨ Enable interrupts on FIFO full
HIEN ⇨ Enable interrupts on FIFO half-full
TIEN ⇨ Enable interrupts on Time Stamp Rollover
IT ⇨ Interrupt Type (0 = Type A (software-end-of-interrupt with vector, RORA), 1 = Type C (hardware-end-of-interrupt with vector, ROAK)
IE ⇨ Interrupt Request Enable (1 = enable interrupts - for Type C interrupts, this bit is automatically cleared during an interrupt acknowledge cycle)
PAT ⇨ Enable pattern recognition for input interrupts (1 = interrupt on a bit pattern, 0 = interrupt on individual bit changes, see Channel Interrupt Enable Register)
Interrupt Vector ⇨ Value presented during interrupt acknowledge cycle

Note: IE must be set to a 1 for any interrupts to occur. When using Type C interrupts (IT = 1), the IE bit is automatically cleared during the interrupt acknowledge cycle and must be re-set at the end of the interrupt service handling routine.

Debounce Control Register

06

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Debounce 12-15				Debounce 8-11				Debounce 4-7				Debounce 0-3			
Read	Debounce 12-15				Debounce 8-11				Debounce 4-7				Debounce 0-3			

Debounce X-Y ⇨ Debounce time for each group of inputs

Slow (DC = 0, see Reg. 00)

Hex	Time	Hex	Time	Hex	Time	Hex	Time
0	0 s	4	64µs	8	1ms	C	16ms
1	8µs	5	128µs	9	2ms	D	32ms
2	16µs	6	256µs	A	4ms	E	64ms
3	32µs	7	512µs	B	8ms	F	128ms

Fast (DC = 1, see Reg. 00)

Hex	Time	Hex	Time	Hex	Time	Hex	Time
0	0 s	4	1.6µs	8	25.6µs	C	410µs
1	200ns	5	3,2µs	9	51.2µs	D	819µs
2	400ns	6	6.4µs	A	102µs	E	1.64ms
3	800ns	7	12.8µs	B	205µs	F	3.28ms

Polarity Register

08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Read	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P15-0 ⇨ Polarity (0 = input not inverted (false (0) = low or open), 1 = input inverted (true (1) = low or open))

Figure 5. I/O Registers (continued)

Watch Register

0A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0
Read	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0

W15-0 ⇨ Watch channel (1 = any change on this channel causes data storage, 0 = ignore changes on channel)

Channel Interrupt Enable Register

0C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Read	IE15	IE14	IE13	IE12	IE11	IE10	IE9	IE8	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0

IE15-0 ⇨ Enable Interrupt (1 = enable interrupt on this channel, 0 = disable or treat this bit as a don't care)

Interrupt Definition Register

0E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Read	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID15-0 ⇨ When PAT = 0 (see Master Interrupt Control Register), 0 = interrupt on any change-of-state, 1 = interrupt only on false to true transition.
When PAT = 1, interrupt on the bit pattern specified (the Channel Interrupt Enable Register specifies don't care bits, 0 = don't care).

Interrupt Pending/Clear Register

10

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0*
Read	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0*

C15-0 ⇨ Clear Interrupt (writing a 1 clears a pending interrupt on this channel)
IP15-0 ⇨ Interrupt Pending (a 1 = pending interrupt on this channel)

* Note: When PAT = 1 (see Master Interrupt Control Register), only C0 and IP0 are used.

FIFO Data Port Register

12

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read 1	DV	Time Stamp (upper half)														
Read 2	Time Stamp (lower half)															
Read 3	Stored Input Value															

DV ⇨ Data Valid (1 = valid data, 0 = FIFO empty)
Time Stamp ⇨ 31-bit time stamp for stored data value
Stored Data Value ⇨ 16-bit input value

Figure 5. I/O Registers (continued)

Current Value Register

14

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)															
Read	Current Value															

Current Value ⇨ Current state of inputs after debounce and before polarity bit inversion

Last Value Stored Register

16

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)															
Read	Last Stored															

Last Stored ⇨ Last value stored in FIFO

FIFO Unread Count Register

18

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read-only)															
Read	Count															

Count ⇨ Number of time-value pairs that have not been read by the user.

Accessory Module Control Register

1A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Read	AMID				0	0	0	0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

ACS7:0 ⇨ Accessory Module Control (some accessory modules use these bits to control specific functions, see Appendix B through E for details)

AMID ⇨ Accessory Module Identification (installed option number)

Figure 5. I/O Registers (continued)

4. OPERATIONAL DESCRIPTION

The MA203 is a register-based instrument that is controlled through a series of I/O registers described in section 3.4.2. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

4.1. DATA ACQUISITION

Configure the module for data acquisition by selecting the clock source and speed, resetting the FIFO and timestamp, defining when to store data, setting the appropriate debounce amount, configuring trigger operation (if required), and selecting the source of the run signal. After or during data acquisition, the FIFO can be read to retrieve stored time-value pairs.

4.1.1. Sample Clock Source/Speed Selection

The source and speed of the sample clock is controlled through the Clock Control Register. The CLKSEL bits allow you to use the internal clock provided by the MA203 or to use an external signal from either the front panel or the backplane trigger A or B. The internal clock speed is selected using the ICLK bits. To use a trigger signal for the clock, your carrier must support trigger operation.

A prescaler may be used with any of the clock sources by setting the PSC bits. Synchronization of several MA203s can be accomplished by using an external clock source connected individually to each module or by using one the modules internal clocks output to trigger. The COS, TO, and TS bits allow you to output the internal clock of a module to a trigger signal. This trigger signal can then be used as the clock source by all of the MA203's including the module providing the trigger signal.

The maximum speed of the sample clock is 5 MHz; however, some input accessory modules may not be capable of input speeds of this rate due to optocoupler limitations. For details, refer to the specifications for the specific AM104 input accessory module in the appendix of this manual.

4.1.2. FIFO and Timestamp Operation

Before starting data acquisition, the FIFO and timestamp should always be reset by writing a 1 to the RFF and RTS bits in the Control/Status Register. Always stop data acquisition (RUN and RUNSEL = 0) before resetting the FIFO and timestamp. The condition of the FIFO is indicated by the DS, FF, and HF bits. The DS bit is one any time there is unread data stored in the FIFO. The FF bit indicates that the FIFO is or was full and can only be reset by resetting the FIFO (RFF) or resetting the entire module. The HF bit indicates that the FIFO is more than half-full.

The 31-bit timestamp is incremented at the rate of the sample clock. The TSR bit is set if the timestamp rolls over to zero. Clear the TSR bit by writing a 1 to the bit.

4.1.3. Data Storage Definition

The Watch Register defines which input channels will cause data storage. A bit set to a 1 will cause that channel to be watched. The current timestamp and the state of the input channels will be stored any time any of the selected watch channels change state. The state of an input channel may be inverted by setting the appropriate bit in the Polarity Register.

The store-all bit (STA) in the Control/Status Register allows data storage on ever sample clock regardless of the setting of the Watch Register. This bit is typically not used during normal operation.

4.1.4. Input Debounce

The amount of time to debounce the input signals is set in the Debounce Control Register. Note that some accessory modules may have some inherent debounce properties that must be taken into account.

4.1.5. Run Source Selection

The source of the RUN signal is controlled through the Control/Status Register. The RUNSEL bits allow the RUN signal to be software controlled or controlled by an external front panel or trigger signal. To avoid spurious sampling, always set the RUNSEL bits to 000 before setting the desired run source. In addition, always configure the sample clock source and speed, reset the FIFO and timestamp, and define the watch channels and debounce time prior to selecting the run source. The external run source selection allows run synchronization of several MA203s.

4.1.6. Retrieving Data

Data retrieval is provided through a single FIFO Data Port Register. By continuously reading the FIFO register and checking the data valid bit, stored data can be retrieved without accessing any other registers. Figure 5 is a flow model to illustrate the data fetch operation. This register can be read when idle or when running.

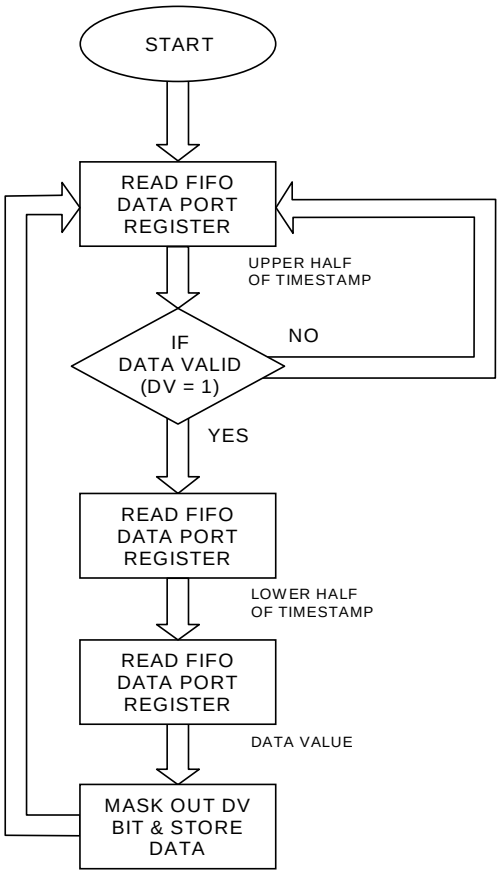


Figure 6. FIFO Data Fetch Operation (Polling Method)

4.2. ACCESSORY MODULE CONTROL

Several accessory modules (AM104s) are available that provide input signal conditioning. These modules are individually described in the appendices of this document starting with Appendix B. Detailed specifications, functional diagrams, programming instructions, and connector pin definitions are provided.

4.3. INTERRUPTS

The MA203 supports Type A and Type C interrupts as specified in the M-module specification. A Type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e., RORA)). A Type C interrupt releases the interrupt request during the interrupt acknowledge cycle (hardware-end-of-interrupt with vector (i.e., ROAK)) Type C interrupts provide an interrupt vector during an interrupt acknowledge cycle. Use the IT bit in the Master Interrupt Control Register to configure the desired type of interrupt.

For any interrupt to occur, the Interrupt Request line must be enabled by writing a one to the IE bit in the Master Interrupt Control Register. The Master Interrupt Control Register is also used to enable data storage status interrupts and to set the interrupt vector. All interrupts use the same interrupt vector. The Channel Interrupt Enable Register is used to enable interrupts due to level changes on a specific input channel.

> NOTE: For any interrupt to occur, the IE bit in the Master Interrupt Control Register must be set.

Data Stored The Data Stored bit (DS bit) is set to a one when any data is stored in the FIFO. It remains a one as long as the FIFO is not empty. Enable an interrupt on this condition by writing a one to the DIEN bit in the Master Interrupt Control Register. Release the interrupt by writing a one to the DS bit in the Control/Status Register. Note that if the FIFO is not empty another interrupt will immediately occur.

FIFO Full The FIFO full bit (FF bit) is set to a one when the FIFO becomes full. The FF bit will remain set until the FIFO is reset by writing a one to the Reset FIFO bit (RFF) in the Control/Status Register or the entire module is reset. Enable an interrupt on this condition by writing a one to the FIEN bit in the Master Interrupt Control Register. Release the interrupt by writing a one to the FF bit in the Control/Status Register. Note that if the FIFO full condition has not been cleared, another interrupt will immediately occur.

FIFO Half Full The FIFO half full bit (HF bit) is set to a one when the FIFO reaches half full. The HF bit will remain set as long as the FIFO is greater than or equal to half full. Enable an interrupt on this condition by writing a one to the HIEN bit in the Master Interrupt Control Register. Release the interrupt by writing a one to the HF bit in the Control/Status Register. Note that if the FIFO half full condition still remains, another interrupt will immediately occur.

Time Stamp Rollover The Time Stamp Rollover (TSR bit) is set to a one when the 31-bit time stamp rolls over to zero. Using this bit and associated interrupt allows software to maintain an infinitely large time stamp. Enable an interrupt on this occurrence by writing one to the TIEN bit in the Master Interrupt Control Register. Release the interrupt by writing a one to the TSR bit in the Control/Status Register.

Change-of-State/Level Channel Interrupts An interrupt can be set to occur when an input changes state (low-to-high or high-to-low) or it transitions to the active state (inactive to active) by setting PAT = 0. The Polarity Register determines the polarity of the active state (high or low) for a given input. The Interrupt Definition Register determines whether an interrupt occurs on any change-of-state or only when the input transitions to the active state. The input causing an interrupt is latched into the Interrupt Pending/Clear Register and only cleared when a 1 is written to that bit. The interrupt request line is only released when no interrupts are pending.

Interrupt On Bit Pattern An interrupt can be set to occur on a specific bit pattern by setting PAT = 1 in the Master Interrupt Control Register. The bit pattern and don't care bits are then specified in the Interrupt Definition and Channel Interrupt Enable Registers, respectfully. When the specified pattern occurs, a pending interrupt is latched into IP0 of the Interrupt Pending/Clear Register and is cleared when a 1 is written to the C0 bit.

4.4. ID PROM

Refer to 3.4.1 M-Module PROM Registers for a description of the ID PROM's function and contents.

The ID PROM is a serial device and involves writing and reading a register in a sequential manner to acquire data. Figure 7 is a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value)
{
   addr = 0xFE;                          /* M/MA address for IDPROM */
   id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
   write_eebyte (addr, id_addr);
   read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
   tmpval = rdval << 8;         /* upper byte of sync code word */
   read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
   tmpval = tmpval | rdval;     /* combine bytes of sync code   */
   *value = tmpval;
   write_word(addr, 0x0000);             /* lower cs */
   return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value)
{

   write_word(addr, 0x0000);             /* insure cs is initially low */
   write_word(addr, 0x0004);             /* initialize */
   write_eebit(addr, 0x0001);            /* start bit */
   temp = value;
   for (i=0;i<=7;i++){
      write_eebit(addr, ((temp & 0x80)>>7));
      temp = (temp << 1);
   }
   return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value)
{
   temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
   write_word(addr, temp);
   Delay(.000005);                       /* delay at least 5us */
   temp = (0x0006 | (value & 0x0001));   /* set data bit & clock */
   write_word(addr, temp);
   Delay(.000005);                       /* delay at least 5us */
   return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value)
{
   for (i=7;i>=0;i=i-1){
      read_eebit (addr, &rdval);
      temp = temp | ((rdval&0x01) << i);
   }
   *value = temp;
   return;
}
/*-------------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value)
{
;
   write_word(addr, 0x4);                /* lower clock bit */
   Delay(.000005);             /* delay at least 5us */
   write_word(addr, 0x6);                /* raise clock bit */
   Delay(.000005);                       /* delay at least 5us */
   read_word (addr, value);
   return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: Functions write_word and read_word are low-level memory access routines that should be replaced with interface specific functions.

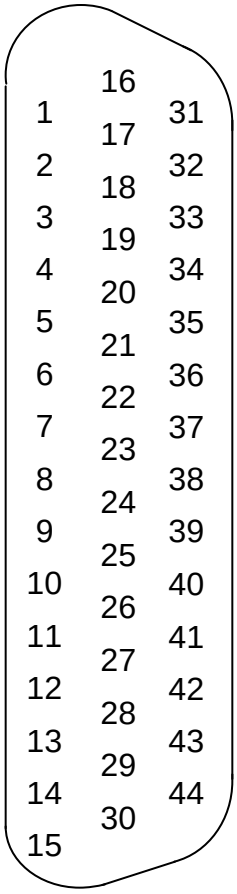
Figure 7. IDPROM Access Routine

APPENDIX A – CONNECTORS

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	(D23)
12	D11	D03/(A11)	(D24)
13	D12	D04/(A12)	(D25)
14	D13	D05/(A13)	(D26)
15	D14	D06/(A14)	(D27)
16	D15	D07/(A15)	(D28)
17	/DS1	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

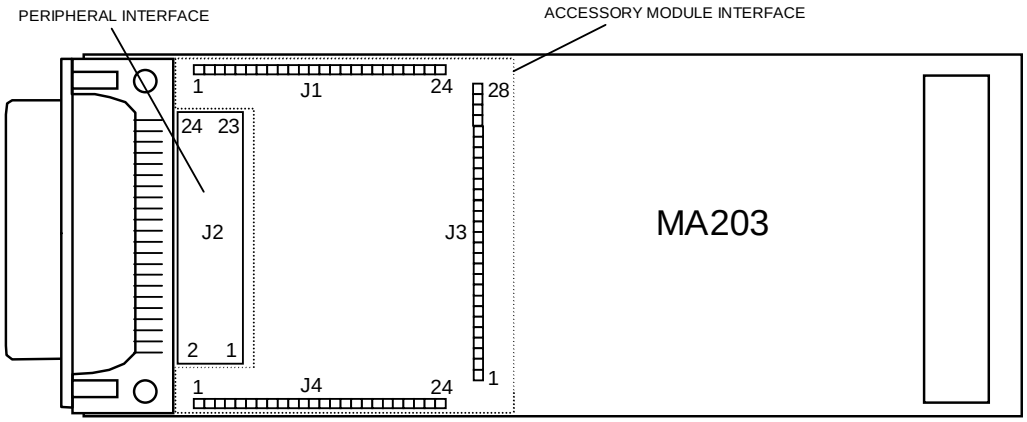
Note: Signals in parentheses ( ) are not used on this module.

Figure A-1. M/MA Interface Connector Configuration



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INA0(+)	16	INB0(-)	31	GND
2	INA1(+)	17	INB1(-)	32	-12VSUP
3	INA2(+)	18	INB2(-)	33	+12VSUP
4	INA3(+)	19	INB3(-)	34	GND
5	INA4(+)	20	INB4(-)	35	ISOVNEG
6	INA5(+)	21	INB5(-)	36	ISOVPOS
7	INA6(+)	22	INB6(-)	37	GND
8	INA7(+)	23	INB7(-)	38	EXTCLK
9	INA8(+)	24	INB8(-)	39	GND
10	INA9(+)	25	INB9(-)	40	EXTRUN
11	INA10(+)	26	INB10(-)	41	GND
12	INA11(+)	27	INB11(-)	42	GND
13	INA12(+)	28	INB12(-)	43	INB15(-)
14	INA13(+)	29	INB13(-)	44	INA15(+)
15	INA14(+)	30	INB14(-)		

Figure A-2. Front Panel D-SUB Connector Configuration



ACCESSORY MODULE INTERFACE

J1				J4				J3			
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INB00	13	INB04	1	INA15	13	INA10	1	GND	15	IN13
2	GND	14	ISOVNEG	2	INB14	14	INB10	2	IN00	16	IN14
3	INA00	15	INA04	3	INA14	15	-	3	IN01	17	IN15
4	INB01	16	INB05	4	INB15	16	INA09	4	IN02	18	AC00
5	-	17	ISOVPOS	5	INB13	17	INB09	5	IN03	19	AC01
6	INA01	18	INA05	6	INA13	18	INA08	6	IN04	20	AC02
7	INB02	19	INB06	7	INA12	19	GND	7	IN05	21	AC03
8	-	20	GND	8	INB12	20	INB08	8	IN06	22	AC04
9	INA02	21	INA06	9	GND	21	+12V	9	IN07	23	AC05
10	INB03	22	INB07	10	INA11	22	-12V	10	IN08	24	AC06
11	GND	23	+5V	11	INB11	23	COMMON	11	IN09	25	AC07
12	INA03	24	INA07	12	GND	24	-	12	IN10	26	LEXTCLK
								13	IN11	27	LEXTRUN
								14	IN12	28	GND

PERIPHERAL INTERFACE

J2			
PIN	SIGNAL	PIN	SIGNAL
1	INA00(+)	2	INB00(-)
3	INA01(+)	4	INB01(-)
5	INA02(+)	6	INB02(-)
7	INA03(+)	8	INB03(-)
9	INA04(+)	10	INB04(-)
11	INA05(+)	12	INB05(-)
13	INA06(+)	14	INB06(-)
15	INA07(+)	16	INB07(-)
17	EXTRUN	18	EXTCLK
19	ISOVPOS	20	-
21	ISOVNEG	22	COMMON
23	GND	24	-

Figure A-3. Accessory Module and Peripheral Interface

APPENDIX B – +5V OPTOCOUPLED INPUT ACCESSORY MODULE (OPT. 1)

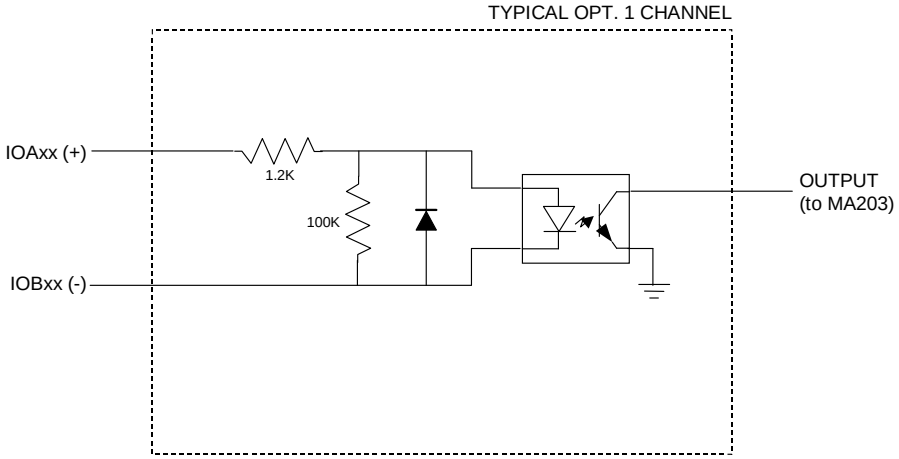
Description

This AM104 accessory module provides an optically coupled input for nominal 0 to +5V signals.

Specifications

Normal Input Voltage Range:	0V to +5V
OFF Input Voltage:	+1.8V (maximum)
ON Input Voltage:	+2.6V (minimum)
Input Protection:	-75V to +28V
Input Resistance:	100KΩ (minimum)
Input Current:	3.5mA per channel at +5V input (maximum)
Input Propagation Delay:	5μs
Maximum Signal Frequency:	200KHz
Channel-Channel Isolation:	10MΩ minimum
Input Voltage Isolation:	1000V minimum

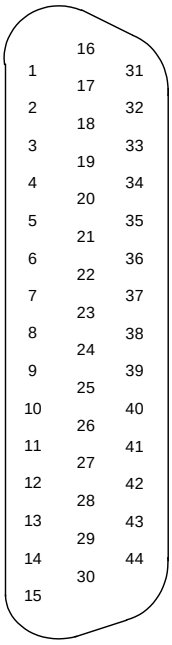
Functional Diagram



Programming

This accessory module does not require any additional programming.

Pin Definitions



AM104 OPT. 1

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INA0(+)	16	INB0(-)	31	GND
2	INA1(+)	17	INB1(-)	32	-12VSUP*
3	INA2(+)	18	INB2(-)	33	+12VSUP*
4	INA3(+)	19	INB3(-)	34	GND
5	INA4(+)	20	INB4(-)	35	ISOVNEG*
6	INA5(+)	21	INB5(-)	36	ISOVPOS*
7	INA6(+)	22	INB6(-)	37	GND
8	INA7(+)	23	INB7(-)	38	EXTCLK
9	INA8(+)	24	INB8(-)	39	GND
10	INA9(+)	25	INB9(-)	40	EXTRUN
11	INA10(+)	26	INB10(-)	41	GND
12	INA11(+)	27	INB11(-)	42	GND
13	INA12(+)	28	INB12(-)	43	INB15(-)
14	INA13(+)	29	INB13(-)	44	INA15(+)
15	INA14(+)	30	INB14(-)		

* These output pins are only used for supplemental operation.

APPENDIX C – +28V OPTOCOUPLED INPUT ACCESSORY MODULE (OPT. 2)

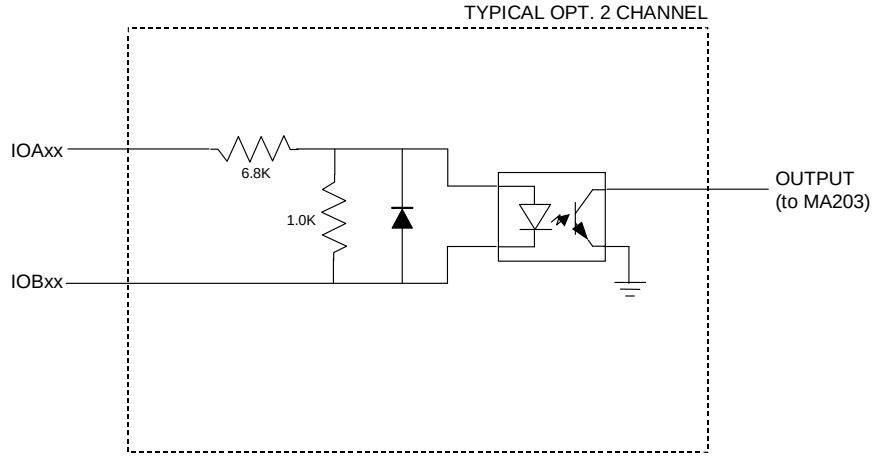
Description

This AM104 accessory module provides an optically coupled input for nominal 0 to +28V signals.

Specifications

Normal Input Voltage Range:	0V to +28V
Maximum OFF Input Voltage:	+11.0V
Minimum ON Input Voltage:	+17.0V
Input Protection:	-75V to +50V
Input Resistance:	7.0KΩ (minimum)
Input Current:	3.0mA per channel at +28V input (maximum)
Input Propagation Delay:	5μs
Maximum Signal Frequency:	200KHz
Channel-Channel Isolation:	10MΩ minimum
Input Voltage Isolation:	1000V minimum

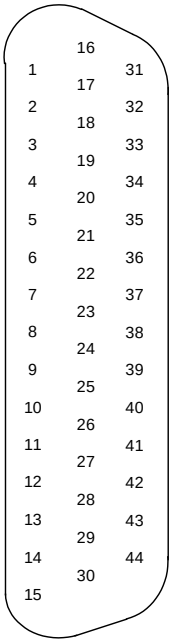
Functional Diagram



Programming

This accessory module does not require any additional programming.

Pin Definitions



AM104 OPT. 2

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INA0(+)	16	INB0(-)	31	GND
2	INA1(+)	17	INB1(-)	32	-12VSUP*
3	INA2(+)	18	INB2(-)	33	+12VSUP*
4	INA3(+)	19	INB3(-)	34	GND
5	INA4(+)	20	INB4(-)	35	ISOVNEG*
6	INA5(+)	21	INB5(-)	36	ISOVPOS*
7	INA6(+)	22	INB6(-)	37	GND
8	INA7(+)	23	INB7(-)	38	EXTCLK
9	INA8(+)	24	INB8(-)	39	GND
10	INA9(+)	25	INB9(-)	40	EXTRUN
11	INA10(+)	26	INB10(-)	41	GND
12	INA11(+)	27	INB11(-)	42	GND
13	INA12(+)	28	INB12(-)	43	INB15(-)
14	INA13(+)	29	INB13(-)	44	INA15(+)
15	INA14(+)	30	INB14(-)		

* These output pins are only used for supplemental operation.

APPENDIX D –CONTACT SENSING INPUT ACCESSORY MODULE (OPT. 3)

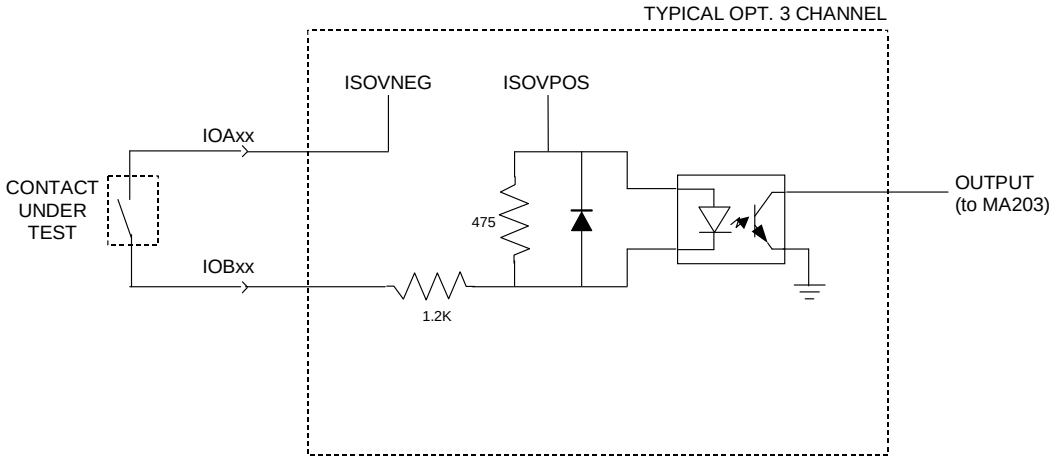
Description

This AM104 accessory module provides an optically coupled contact sensing input for testing the continuity of switch or relay contacts. An on-board isolated supply provides the necessary current for sensing the open or closed status of the contact under test.

Specifications

Output Sensing Current:	3.25ma (typical)
Output Voltage:	+5V (isolated supply from base module)
Maximum OPEN Sense Current:	2.1ma (1000Ω minimum resistance)
Minimum CLOSED Sense Current:	4.4ma (100Ω maximum resistance)
Input Propagation Delay:	5μs
Maximum Signal Frequency:	200KHz

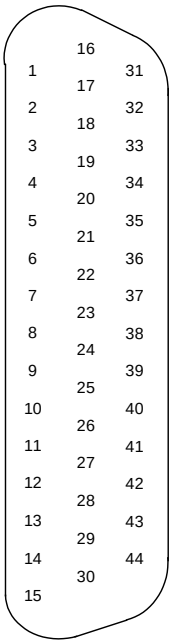
Functional Diagram



Programming

This accessory module does not require any additional programming.

Pin Definitions



AM104 OPT. 3

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INA0(+)	16	INB0(-)	31	GND
2	INA1(+)	17	INB1(-)	32	-12VSUP*
3	INA2(+)	18	INB2(-)	33	+12VSUP*
4	INA3(+)	19	INB3(-)	34	GND
5	INA4(+)	20	INB4(-)	35	ISOVNEG*
6	INA5(+)	21	INB5(-)	36	ISOVPOS*
7	INA6(+)	22	INB6(-)	37	GND
8	INA7(+)	23	INB7(-)	38	EXTCLK
9	INA8(+)	24	INB8(-)	39	GND
10	INA9(+)	25	INB9(-)	40	EXTRUN
11	INA10(+)	26	INB10(-)	41	GND
12	INA11(+)	27	INB11(-)	42	GND
13	INA12(+)	28	INB12(-)	43	INB15(-)
14	INA13(+)	29	INB13(-)	44	INA15(+)
15	INA14(+)	30	INB14(-)		

* These output pins are only used for supplemental operation.

APPENDIX E – PROGRAMMABLE THRESHOLD ACCESSORY MODULE (OPT. 4)

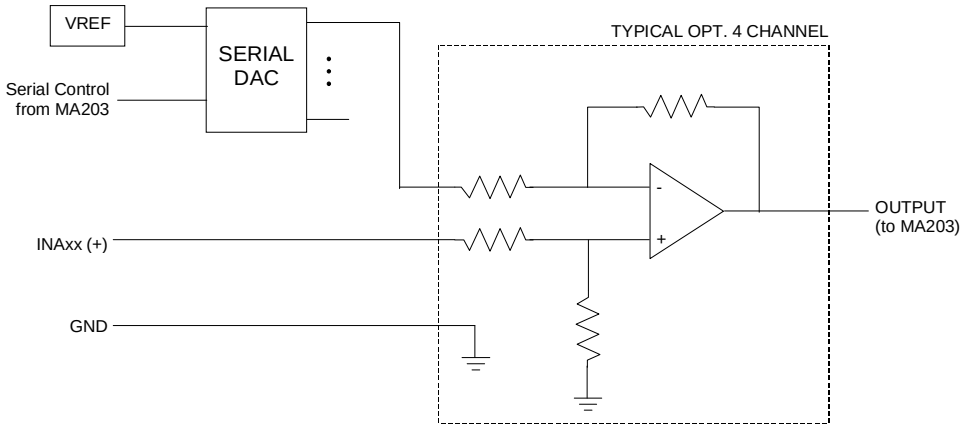
Description

The AM104 Opt. 4 accessory module provides high-speed programmable threshold digital input capability to the MA203. Each input channel is independently programmable.

Specifications

Threshold Programming Range:	0 – 25.5V
Threshold Programming Resolution:	100mV (8-bits)
Threshold Accuracy:	±0.5% of full scale (±127mV)
Threshold Programming:	3-bit Serial
Maximum Input Voltage:	48V
Input Hysteresis:	25mV
Input Impedance:	>100KΩ
Input Current:	<300μA (input voltage ≤ 30V)
Maximum Signal Frequency:	5MHz

Functional Diagram



Programming

The AM104 Opt. 4 Programmable Threshold accessory module must be programmed to set the input threshold of each of the inputs. The module uses two MAX528 octal serial DACs to set the threshold levels. The DAC is serially programmed through the Accessory Module Control Register (1Ah) discussed in section 3.4.2. The DAC's control signals are controlled using the accessory module control bits shown below.

Accessory Module Control Register with AM104 Opt. 4 Installed

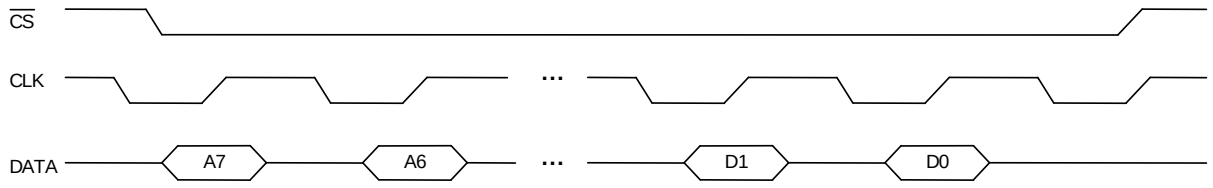
1A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	-	-	-	-	CS1-	CS0-	DATA	CLK
Read	0	1	0	0	0	0	0	0	-	-	-	-	CS1-	CS0-	DATA	CLK

CS1- ⇨ DAC Chip Select for channels 8-15
CS0- ⇨ DAC Chip Select for channels 0-7
DATA ⇨ Serial Data to DAC (write only)
CLK ⇨ Serial Clock to DAC

The input threshold is programmed by sending a 16 bit instruction to the DAC. The programming data must consist of 8 address bits followed by 8 data bits. Each address bit (A7-A0) selects an input channel, so any combination of 8 channels can be programmed simultaneously. The proper chip select line must be asserted (CS0- or CS1- = 0) to address the corresponding input channels. CS0- addresses channels 0-7 while CS1- addresses channels 8-15. The 8 data bits (D7-D0) represent the input threshold level that the addressed channels are programmed to. Each bit is equal to 100mV allowing for a programming range of 0-25.5V.

The programming sequence is illustrated in the following figure.



Programming Sequence

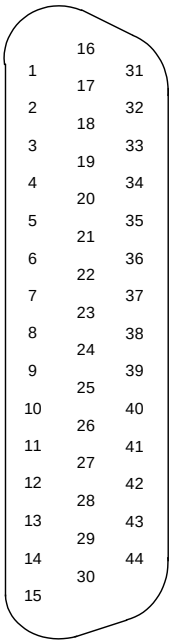
For proper operation both DAC's must be set to full-buffered mode. This is achieved using the same programming sequence illustrated in the above figure, with all address bits equal to 0 and the data bits equal to FFh.

The following example code is a general description of how to program the input threshold and how to set the DAC's into full buffered mode.

```
/*-------------------------------------------------------------------------*/
int init_am104_option4()
{  write_dac(0, 0x00FF);                          /* set DAC 0 to full buffered */
   write_dac(1, 0x00FF);                          /* set DAC 1 to full buffered */
}
/*-------------------------------------------------------------------------*/

int set_input_threshold(unsigned short channel_mask, unsigned short volts)
{  unsigned short data = 0;

   data = (volts/0.1);                            /* 100mV resolution */

   if((channel_mask & 0xFF) != 0)
   {  data |= (channel_mask & 0xFF) << 8;
      write_dac(0, data);                         /* set channels 0-7 */
   }

   if((channel_mask & 0xFF00) != 0)
   {  data &= 0x00FF;
      data |= channel_mask & 0xFF00;
      write_dac(1, data);                         /* set channels 8-15 */
   }

   return 0;
}
/*-------------------------------------------------------------------------*/

int write_dac(int chip_select, unsigned short data)
{  unsigned short reg_data;
   int i;

   read_word(MA203_ACC_REG_ADDR, &reg_data);

   reg_data |= 0xC;                               /* raise both chip selects */
   write_word(MA203_ACC_REG_ADDR, reg_data);

   reg_data &= ~0x1;                              /* lower clock */
   write_word(MA203_ACC_REG_ADDR, reg_data);

   reg_data &= ~(0x1 << (2 + chip_select));       /* lower chip select */
   write_word(MA203_ACC_REG_ADDR, reg_data);

   for(i=0; i<16; i++)
   {  if(data & 0x8000)                           /* set DATA */
        reg_data |= 0x2;
      else
        reg_data &= ~0x2;
      write_word(MA203_ACC_REG_ADDR, reg_data);

      reg_data |= 0x1;                            /* raise CLK */
      write_word(MA203_ACC_REG_ADDR, reg_data);

      reg_data &= ~0x1;                           /* lower CLK */
      write_word(MA203_ACC_REG_ADDR, reg_data);

      data <<= 1;
   }
   reg_data |= (0x1 << (2 + chip_select));        /* raise chip select */
   write_word(MA203_ACC_REG_ADDR, reg_data);

   return 0;
}

/*-------------------------------------------------------------------------*/
```

NOTE: Functions write_word and read_word are low-level memory access routines that should be replaced with interface specific functions.

Pin Definitions



AM104 OPT. 4

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	INA0(+)	16	GND	31	GND
2	INA1(+)	17	GND	32	-12VSUP*
3	INA2(+)	18	GND	33	+12VSUP*
4	INA3(+)	19	GND	34	GND
5	INA4(+)	20	GND	35	ISOVNEG*
6	INA5(+)	21	GND	36	ISOVPOS*
7	INA6(+)	22	GND	37	GND
8	INA7(+)	23	GND	38	EXTCLK
9	INA8(+)	24	GND	39	GND
10	INA9(+)	25	GND	40	EXTRUN
11	INA10(+)	26	GND	41	GND
12	INA11(+)	27	GND	42	GND
13	INA12(+)	28	GND	43	GND
14	INA13(+)	29	GND	44	INA15(+)
15	INA14(+)	30	GND		

* These output pins are only used for supplemental operation.

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