****** IMPORTANT ******

ERRATA INFORMATION
MAY 2002

This erratum contains important information for proper operation of the following product.

Product: MA201 24-Channel Driver MA-Module

Manual Edit:

- WARNING -

Do not apply power to the external power signals (Vhi and Vlo) on the front panel connectors until after the MA201 is powered on. Turning on the MA201 while the external power is present could potentially damage the module.

U S E R ' S M A N U A L

24 CHANNEL DRIVER
MA-MODULE

MODEL
MA201

Document Part No: 11027964

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NOTE

The contents of any amendment may affect operation, maintenance, or calibration of the equipment.

INTRODUCTION

This manual describes the operation and use of the C&H Model MA201 MA-Module (Part Number 11027960). This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as VME, VXI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

Part numbers covered by this manual are:

Part Number	Description
11027960-0003	24 channels, 30-150 volts
11027960-0004	24 channels, 25-130 volts
11027960-0005	24 channels, 20-100 volts
11027960-0006	24 channels, 15-70 volts
11027960-0007	24 channels, 10-50 volts
11027960-0008	24 channels, 5-25 volts

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1.0 GENERAL DESCRIPTION

The MA201 is a 24 channel driver capable of sequentially driving each of the 24 channels at levels up to 150 volts. The module monitors and records, on-the-fly, the high and low voltage levels and the currents being drawn by the high and low drivers. This information is recorded into on-board memory. Alarm limits may be preprogrammed for any of these values to facilitate interrupts or safety shut-downs. Synchronization with multiple modules is possible.

The module is physically implemented on a doublewide M/MA-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules, which allows it to operate in any system for which an M-Module carrier is available. Carriers are currently available in VXI, VME, PC, cPCI, and many other formats.

1.1 PURPOSE OF EQUIPMENT

The MA201 provides 24 channels of high voltage drive and monitor capability. It can be used in a wide variety of applications including field emissions device testing, high voltage display testing, high voltage automotive testing, high voltage digital input testing, or in any application requiring a multi-channel sequential source.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- 24 Channels: Sequentially driven
  Programmable on/off times
- High Voltage Rail: Up to 150 VDC depending on option
- Low Voltage Rail: Ground
- Sink or Source Current: 200mA per channel
- 12-bit A/D Measurements: High Voltage Rail
  Low Voltage Rail
  Current drawn by all high drivers
  Current drawn by all low drivers
  Control lines for two external 12-bit A/D modules
- Memory: 32Kx8 SRAM
- Programmable Alarms: Vhi max and min
  Vlo max and min
  Ihi max and min
  Ilo max and min
  Ext 1 max and min
  Ext 2 max and min
- Over Current Protection: Automatic shut-down
- Synchronization: 4 M-module trigger lines

1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +70	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V	1.0 max.	A
	+12V	0.2 max.	A
	-12V	0.2 max.	A
Supply Voltage (Vhi)	-0003 no damage	150 max	VDC
	-0004 no damage	130 max	VDC
	-0005 no damage	100 max	VDC
	-0006 no damage	70 max	VDC
	-0007 no damage	50 max	VDC
	-0008 no damage	25 max	VDC

AC CHARACTERISTICS

		Limit			
Parameter	**Conditions**	**Min**	**Typ.**	**Max**	**Units**
Driver Characteristics					
Channel Output					
- Voltage Range[1]	-0003	30		150	V
	-0004	25		130	V
	-0005	20		100	V
	-0006	15		70	V
	-0007	10		50	V
	-0008	5		25	V
- Current				200	mA
- Constant Level Maximum[2]	-0003			46	V
	-0004			44	V
	-0005			39	V
	-0006			35	V
	-0007			32	V
	-0008			25	V
Dynamic Performance					
Pulse Period					
- Programming Range[3]	Internal period control	1		65,535	µsec
- Programming Resolution	Internal period control		1		µsec
- Functional Range[3]	Maintain integrity of A/D measurements	36		65,535	µsec
Snapshot Delay					
- Programming Range	Internal snapshot control	1		255	µsec
- Programming Resolution	Internal snapshot control		1		µsec
Over-current Bypass[4]					
- Programming Range		0		15	µsec
- Programming Resolution			1		µsec
Channel Sequence					
- Start Channel	Start Channel < End Channel	1		24	Ch. #
- End Channel	Start Channel < End Channel	1		24	Ch. #

AC CHARACTERISTICS (continued)

Parameter	Conditions	Limit Min	Typ.	Max	Units
Measurement Capabilities					
Snapshots					
- Volatile Memory			32K		bytes
- Num Bytes per Snapshot			13		bytes
- Num Total Snapshots				20,164	snapshots
- Snapshot Meas. Time[3]				35	μsec
- A/D Acquisition Time[5]				1.5	μsec
Vhi					
- Range		0		150	V
- Resolution			51		mV
Vlo					
- Range		0		82	V
- Resolution			20.1		mV
Ihi					
- Range		0		200	mA
- Resolution			49.1		μA
Ilo					
- Range		0		200	mA
- Resolution			49.1		μA
External A/D Control					
- Size			12		bits
- Recommended A/D	MAX187 - 12-bit A/D, 3-wire serial intf.				
Alarm Limits					
Vhi					
- Programming Range		0		150	V
- Programming Resolution			816		mV
Vlo					
- Programming Range		0		82	V
- Programming Resolution			322		mV
Ihi					
- Programming Range		0		200	mA
- Programming Resolution			785		μA
Ilo					
- Programming Range		0		200	mA
- Programming Resolution			785		μA
External A/D					
- Programming Range			8[6]		bits
Over Current Protection					
Over Current Threshold					
- Level			210		mA

Notes:

1. The voltage range in which the drivers can source up to 200mA. Below this minimum the drive capability rapidly diminishes. The maximum voltage must not be exceeded or the module may be damaged.
2. The highest voltage level that can be constantly driven by a channel without damaging the module. Higher voltage should only be driven while the channels are pulsing.
3. Snapshot measurements take a maximum of 35 μsec to complete. The MA201 can be programmed for a step period of less than 35 μsec, however the A/D measurements will not be valid.
4. Over-current protection is disabled during a programmable bypass time after each change of driver state. This facilitates ignoring current spikes caused by driver switching.
5. The internal A/D's take a maximum of 1.5 μsec to capture the signal after the snapshot signal goes active. Once acquired, another 5.5–8.5 μsec is required to perform the conversion.
6. Upper 8 bits of a 12 bit A/D value.

1.2.3 Electrical

The MA201 requires the +5V and ±12V power from the M-Module carrier.

1.2.4 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for doublewide M-Module modules. The nominal dimensions are 5.837" (148.26 mm) long × 4.183" (106.24 mm) wide.

1.2.5 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +50°C
Storage Temperature:	-40°C to +70°C
Humidity:	<95% without condensation

Carrier modules may differ in environmental specification. Refer to the carrier's documentation for information.

1.2.6 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for doublewide M-Modules and the MA-Module trigger signal extension.

Module Type:	MA-Module
Addressing:	A08
Data:	D8
Interrupts:	INTA
DMA:	Not Supported
Triggers:	TRIGI, TRIGO
Identification:	Not Supported

1.2.7 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the MA201 is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The MA201 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M-MODULES

> CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

All M-Modules must be installed into the carrier before the carrier is installed into the host system. M-Modules are installed by firmly pressing the connector on the M-Module together with the connector on the carrier. Secure the M-Module with mounting hardware provided as shown in Figure 1.

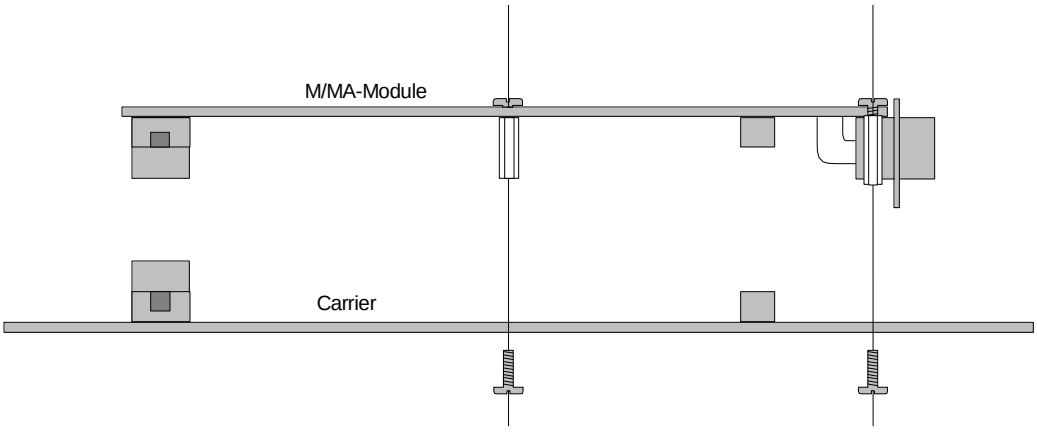


Figure 1. M-Module Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The MA201 provides 24 high voltage channels than can be sequentially driven and sampled at levels up to 150 volts. On-board A/D converters can measure the high voltage rail, the low voltage rail, the current drawn by the high driver, and the current drawn by all low drivers at each step in the sequence. Control signals for two external A/D converters are also provided at the front panel connector. Over current protection circuitry exists that will shut down the drivers if an over current condition is met. A/D data is stored in 32 Kilobytes of on-board SRAM to be read through the M-Module interface. Minimum and Maximum alarm limits can be set for each A/D converter to facilitate interrupts and safety shutdowns. Synchronization with other modules is possible through the M-module trigger lines. A simplified block diagram of the module is shown in Figure 2.

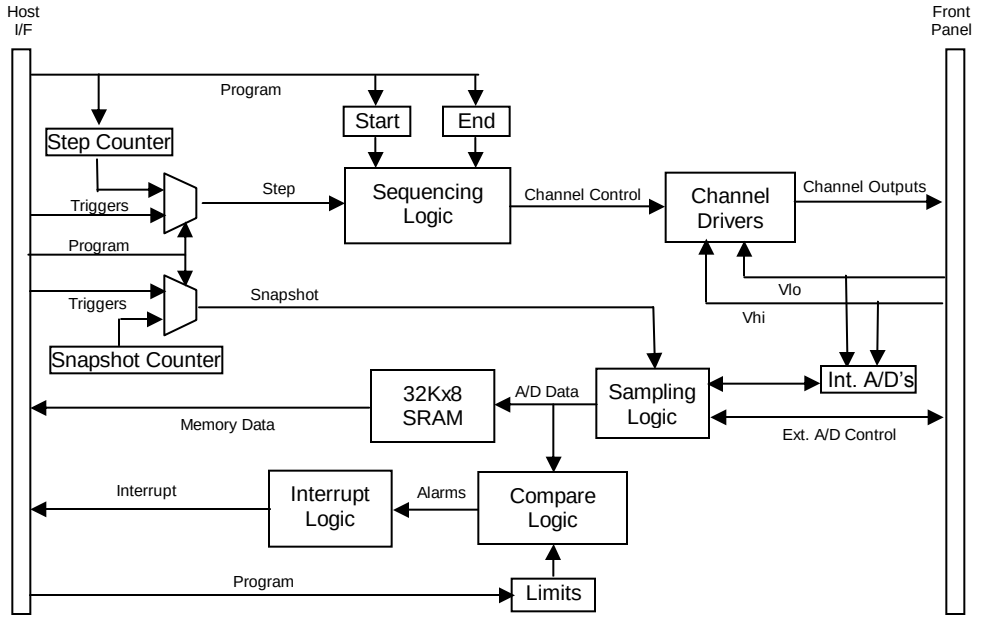


Figure 2. Functional Block Diagram

3.1.1 24 Channel Drivers

Each of the 24 channel drivers can sink or source up to 200mA throughout its voltage range. The voltage range of the drivers is determined by the option number of the module and can range as high as 150V. Refer to the specifications in section 1.2.2 for the voltage range of each option. The driver levels are determined by the external power provided to the drivers through the front panel I/O connector. The low voltage rail (Vlo) must be connected to the ground reference of the external power supply.

3.1.2 Sequencing Logic

The sequencing logic controls the on/off state of the channel drivers. When the card is running, the module will sequence from the start channel to the end channel at a rate determined by an internal step signal. The step signal can come from any of the 4 M-module trigger lines, from a software trigger, or from an internal programmable counter. If the module is in continuously cycle mode then the logic will repeat the sequence until it is programmed to stop. In single cycle mode the module will step through the sequence once then stop.

3.1.3 A/D Sampling

The MA201 has four internal A/D converters and control lines for two external A/D converters. At each step in the sequence the module will sample all six A/Ds and store the data, called a snapshot, into memory. The four internal A/D's measure the high voltage rail (Vhi), the low voltage rail (Vlo), the current drawn by the high driver (Ihi), and the current drawn by all low drivers (Ilo). Snapshots are triggered by an internal snapshot signal. The snapshot signal can originate from an internal programmable counter or from any of the 4 M-module trigger lines.

The external A/D interfaces where designed to interface with the MAX187 12-bit serial A/D from Maxim Integrated Products. The MAX187 features a high speed 3-wire serial interface. Refer to the MAX187 data sheet for more information on this interface.

3.1.4 Memory

The module contains 32 Kilobytes of SRAM memory. The memory is used to store A/D snapshot data and can be accessed through the cards I/O space. A single snapshot requires 13 bytes of memory for storage. Therefore a total of 2520 snapshots can be stored at once. When memory is full the MA201 wraps its memory pointer and continues storing so that the memory always contains the most recent 2520 snapshots.

3.1.5 Compare Logic

At each step in the sequence the data from each A/D converter will be compared to a set of limits that can be programmed through the MA201 I/O registers. If the A/D data is outside the programmed limits a flag will be set and, if enabled, an interrupt will be generated.

3.1.6 Over Current Protection

The over current protection logic monitors the current drawn or sourced by the high channel and all the low channels. If the current exceeds the over current protection threshold all drivers will be immediately disabled and an interrupt request will be generated. Over current protection is on at all times except for a programmable bypass period after a driver changes states. Programmable controls allow the user to enable or disable the over current protection interrupt.

3.2 HARDWARE CONFIGURATION

There are no hardware configurable controls for this module.

3.3 CONNECTORS

3.3.1 M-Module Logic Bus Connector

The M-Module logic bus connector contains signal and voltage connections for the M-Module interface logic. (See Appendix A for pin assignments)

3.3.2 I/O Connectors

The front panel I/O connectors consist of two standard 25-pin D-subminiature male receptacles (AMP Part # 747842-6). The signals and functional descriptions provided on the connectors are as follows (See Appendix A for pin assignments):

CH1 to CH24	Channel Driver Output
Vhi	High Voltage Rail Input
Vlo	Low Voltage Rail Input
AD5CS-	External A/D Chip Select
AD5CLK-	External A/D Clock
AD5DATA-	External A/D Data Line
AD6CS-	External A/D Chip Select
AD6CLK-	External A/D Clock
AD6DATA-	External A/D Data Line
+12VDC	+12V supply (do not exceed 100mA)
-12VDC	-12V supply (do not exceed 100mA)
+5VDC	+5V supply (do not exceed 500mA)
GND	Digital Logic Ground

Note: During normal operation Vlo must be tied to the ground reference of the external power supply.

3.3.3 M-Module Peripheral Connectors

The M-Module peripheral connectors allow connection of certain I/O signals to carrier boards that support this option (See Appendix A for pin assignments).

3.4 CONFIGURATION REGISTERS

3.4.1 IO Registers

There are a variety of registers used to configure and control the MA201 module. The registers are addressable within the I/O space. The MA201 only supports 8-bit reads and writes to I/O space. However, all registers are implemented using the odd bytes of the modules I/O space to facilitate 16-bit word addressing. If a 16-bit read or write is performed, the even byte is simply ignored by the module. An address map of the registers is shown in Table I. The registers provide control, status, memory access, sequence configuration, multiple module synchronization, and alarm configuration. Details of the registers are provided in Figure 3.

Table I. I/O Address Map

IO Address (hex)	Register Description
01	Control/Status
03	Snapshot Data
05	Memory Address MSB
07	Memory Address LSB
09	Bypass
0B	Snapshot Time
0D	Total Num Channels +1
0F	Sequence
11 thru 23	Reserved
25	Step Control
27	Snapshot Control
29	Misc. Sync Control
2B	Step Time MSB
2D	Step Time LSB
2F	Channel End
31	Channel Start -1
33 thru 3B	Reserved
3D	Interrupt Enable MSB
3F	Interrupt Enable LSB
41	Vhi Maximum
43	Vhi Minimum
45	Vlo Maximum
47	Vlo Minimum
49	Ihi Maximum
4B	Ihi Minimum
4D	Ilo Maximum
4F	Ilo Minimum
51	External 1 Maximum
53	External 1 Minimum
55	External 2 Maximum
57	External 2 Minimum
59	Interrupt Pending MSB
5B	Interrupt Pending LSB
5D	Channel Number -1
5F	Revision

Control/Status Register (01_{16}) This read/write register provides the main control of the module operation. Bits are provided to control run, step, cycle mode, interrupt enable, interrupt pending, and output inversion.

Snapshot Data Register (03_{16}) This read-only register contains the snapshot data read from memory. Each read to the register will fetch data from the memory location addressed by the User Pointer. The User Pointer is auto-incremented on a read of this register.

Memory Address MSB Register (05_{16}) This read/write register controls the two internal memory pointers. A read of this register returns the Most Significant Byte (MSB) of the A/D Memory Pointer. A write to this register will write to the MSB of the User Memory Pointer.

Memory Address LSB Register (07_{16}) This read/write register controls the two internal memory pointers. A read of this register return the Least Significant Byte (LSB) of the A/D Memory Pointer. A write to this register will write to the LSB of the User Memory Pointer.

Bypass Register (09_{16}) This read/write register contains timing control for the high current detect during driver state changes. The Bypass time gates off the high current detect inputs for a period after drivers are switched.

Snapshot Time Register ($0B_{16}$) This read/write register defines how long after the sequence is stepped that a snapshot is taken. This time period is only used if the module is programmed to use the internal snapshot signal. The resolution is 1μs/Bit.

Total Num Channels +1 Register ($0D_{16}$) This read/write register contains the total number of channels to be used for all cascaded cards. If multiple cards are cascaded this value is used to determine where in the overall sequence this module's channel sequence lies. If the module is used by itself then this value must be equal to the number of channels +1 programmed for this card only.

Sequence Register ($0F_{16}$) This read/write register is used to determine where in the overall sequence of cascaded cards this module's channel sequence lies. If the module is used by itself then this value should be set to 1.

Step Control Register (25_{16}) This read/write register provides control over the source of the step signal. The step signal can be programmed to come from the internal step counter, the step bit, or any of the 4 backplane trigger lines. Bits are also provided to output the step signal to any of the 4 trigger lines.

Snapshot Control Register (27_{16}) This read/write register provides control over the source of the snapshot signal. The snapshot signal can be programmed to come from the internal snapshot counter or any of the 4 backplane trigger lines. Bits are also provided to output the snapshot signal to any of the 4 trigger lines.

Misc. Sync Control Register (29_{16}) This read/write register provides control over some of the miscellaneous synchronization tools provided by the module. Specifically bits are provided to output an End of Sequence (EOS) signal to any of the 4 trigger lines.

Step Time MSB Register ($2B_{16}$) This read/write registers controls the period of the internal step signal. This time period is only used if the module is programmed to use the internal step signal. The resolution is 1μs/Bit.

Step Time LSB Register ($2D_{16}$) This read/write registers controls the period of the internal step signal. This time period is only used if the module is programmed to use the internal step signal. The resolution is 1μs/Bit.

Channel End Register ($2F_{16}$) This read/write register programs the last channel to be activated in the sequence.

Channel Start -1 Register (31_{16}) This read/write register programs the first channel (-1) to be activated in the sequence.

Interrupt Enable MSB Register ($3D_{16}$) This read/write register individually enables the different types of interrupts requests available.

Interrupt Enable LSB Register ($3F_{16}$) This read/write register individually enables the different types of interrupts requests available.

Vhi Maximum Register (41_{16}) This read/write register programs the maximum high voltage limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Vhi Minimum Register (43_{16}) This read/write register programs the minimum high voltage limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Vlo Maximum Register (45_{16}) This read/write register programs the maximum low voltage limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Vlo Minimum Register (47_{16}) This read/write register programs the minimum low voltage limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Ihi Maximum Register (49_{16}) This read/write register programs the maximum high side current limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Ihi Minimum Register ($4B_{16}$) This read/write register programs the minimum high side current limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Ilo Maximum Register ($4D_{16}$) This read/write register programs the maximum low side current limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Ilo Minimum Register ($4F_{16}$) This read/write register programs the minimum low side current limit. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

External 1 Maximum Register (51_{16}) This read/write register programs the maximum limit for the external A/D input number 1. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

External 1 Minimum Register (53_{16}) This read/write register programs the minimum limit for the external A/D input number 1. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

External 2 Maximum Register (55_{16}) This read/write register programs the maximum limit for the external A/D input number 2. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

External 2 Minimum Register (57_{16}) This read/write register programs the minimum limit for the external A/D input number 2. If this limit is exceeded the corresponding interrupt pending bit will be set and, if enabled, an interrupt request will be generated.

Interrupt Pending MSB Register (59_{16}) This read-only register and register $5A_{16}$ contain the interrupt pending/status bits for all available limits and the high current detect interrupt.

Interrupt Pending LSB Register ($5B_{16}$) This read/write register and register 58_{16} contain the interrupt pending/status bits for all available limits and the high current detect interrupt. A write to this register will clear all interrupt requests except for the high current select interrupt which can only be cleared on a reset.

Channel Number -1 Register ($5D_{16}$) This read-only register contains the channel number (-1) that is currently being driven. If the module is idle this register contains the last channel number (-1) that was driven when the module was stopped.

Revision Register ($5F_{16}$) This read-only register contains the revision level of the on-board digital logic.

Control/Status

01

Bit	7	6	5	4	3	2	1	0
Write	INV	CYC	RST MEM	STEP	RST	-	MIEN	RUN
Read	INV	CYC	WRAP	-	0	MIPEN	MIEN	RUN

RUN ⇨ Run (0 = All drivers off, 1 = Sequence from start to end using step signal) [1]
MIEN ⇨ Master Interrupt Enable (0 = Interrupts disabled, 1 = Interrupts enabled)
MIPEN ⇨ Master Interrupt Pending (0 = No interrupt pending, 1 = Interrupt pending)
RST ⇨ Reset (1 = reset) [2]
STEP ⇨ Step (If SEQSEL = 0001_8 and RUN = 1, writing a 1 to this bit will step the sequence)
WRAP ⇨ Wrap (1 = A/D Pointer wrapped, 0 = A/D Pointer did not wrap)
RST MEM ⇨ Reset Memory (1 = reset A/D Pointer to 0)
CYC ⇨ Cycle Mode (0 = Continuous Cycle, 1 = Single Cycle)[1]
INV ⇨ Invert Channel Outputs (1 = Inverted outputs, 0 = Non-inverted outputs)

Notes:
1. When in single cycle mode (CYC = 1) the RUN bit will automatically be cleared at the end of the sequence
2. Reset is the only way to recover from an over current condition.

Snapshot Data

03

Bit	7	6	5	4	3	2	1	0
Write	(read only)							
Read	Snapshot Data							

Snapshot Data ⇨ 1 byte of snapshot data read from the address pointed to by the user memory pointer set using the Memory Address Registers (05_{16} & 07_{16}). The user memory pointer will be auto-incremented. Refer to section 4.3 for details on reading snapshots.

Memory Address MSB

05

Bit	7	6	5	4	3	2	1	0
Write	User Pointer MSB							
Read	A/D Pointer MSB							

Memory Address LSB

07

Bit	7	6	5	4	3	2	1	0
Write	User Pointer LSB							
Read	A/D Pointer MSB							

User Pointer ⇨ Sets the memory address from which snapshot data is read from on a read of the Snapshot Data Register (03_{16}). The User Pointer is auto-incremented on a read of the Snapshot Data register (03_{16}). Refer to section 4.3 for details on reading snapshots.
A/D Pointer ⇨ The current address at which the module is storing A/D snapshots

Figure 3. I/O Registers

Bypass

09 Bit	7	6	5	4	3	2	1	0
Write	-	-	-	-	Bypass (1µs/Bit)			
Read	-	-	-	-	Bypass (1µs/Bit)			

Bypass (1µs/Bit) ⇨ Inhibits the high current detect for the amount of micro-seconds indicated by this binary number. This inhibit is enabled each time a driver changes state.

Snapshot Time

0B Bit	7	6	5	4	3	2	1	0
Write	Snapshot Time (1µs/Bit)							
Read	Snapshot Time (1µs/Bit)							

Snapshot Time (1µs/Bit) ⇨ The delay before a snapshot is taken at each step in the sequence. It should be typically set for a time that allows for the driver outputs to settle. This register is only used if the source of the snapshot signal is set to Internal (Snapshot Control Register (27_{16}) Bits 0-3 = 0_{16})

Note: There is a finite amount of time between when the snapshot signal goes active and when the A/D converters actually acquire the signals. Refer to the A/D Acquisition Time specification in section 1.2.2 for details.

Total Num Channels + 1

0D Bit	7	6	5	4	3	2	1	0
Write	Total Num Channels + 1							
Read	Total Num Channels + 1							

Total Num Channels ⇨ The total number of channels (+1) for all cascaded modules. If multiple modules are being cascaded this register along with the Sequence Register ($0F_{16}$) determines where in the overall sequence this module's channels lie. Refer to section 4.6 for details on cascading and synchronizing multiple cards.

Figure 3. I/O Registers (continued)

Sequence

0F Bit	7	6	5	4	3	2	1	0
Write	Sequence Number							
Read	Sequence Number							

Sequence Number ⇨ Defines where this driver's first channel sits in the sequence of channels for all driver cards. Typically it will be set to a binary one (1) unless multiple cards are to be cascaded. Refer to section 4.6 for details on synchronizing multiple cards.

Step Control

25 Bit	7	6	5	4	3	2	1	0
Write	-	STEPOUT			STEPSEL			
Read	-	STEPOUT			STEPSEL			

STEPSEL ⇨ Step Select (Selects the source of the sequence step signal)

	Rising Edge		Falling Edge
0000	Internal (default)	0001	Step Bit
0010	Backplane Trigger A	0011	Backplane Trigger A
0100	Backplane Trigger B	0101	Backplane Trigger B
0110	Backplane Trigger C	0111	Backplane Trigger C
1000	Backplane Trigger D	1001	Backplane Trigger D
1010	(reserved)	1011	(reserved)
1100	(reserved)	1101	(reserved)
1110	(reserved)	1111	(reserved)

STEPOUT ⇨ Step Output (Output the step signal)

0 0 0	None (default)
0 0 1	Backplane Trigger A
0 1 0	Backplane Trigger B
0 1 1	Backplane Trigger C
1 0 0	Backplane Trigger D

Note: Refer to section 4.6 for details on synchronizing multiple cards.

CAUTION: The maximum voltage specifications are only valid when the sequence is running. When using a step select setting other than "Internal" verify that the step signal is running before providing a voltage higher than the constant level maximum specification.

Figure 3. I/O Registers (continued)

Snapshot Control

27

Bit	7	6	5	4	3	2	1	0
Write	-	SNAPSHOT OUT			SNAPSHOT SEL			
Read	-	SNAPSHOT OUT			SNAPSHOT SEL			

SNAPSHOT SEL ⇨ Snapshot Select (Selects the source of the snapshot signal)

	Rising Edge		Falling Edge
0000	Internal (default)	0001	(reserved)
0010	Backplane Trigger A	0011	Backplane Trigger A
0100	Backplane Trigger B	0101	Backplane Trigger B
0110	Backplane Trigger C	0111	Backplane Trigger C
1000	Backplane Trigger D	1001	Backplane Trigger D
1010	(reserved)	1011	(reserved)
1100	(reserved)	1101	(reserved)
1110	(reserved)	1111	(reserved)

SNAPSHOT OUT ⇨ Snapshot Output (Output the snapshot signal)

0 0 0	None (default)
0 0 1	Backplane Trigger A
0 1 0	Backplane Trigger B
0 1 1	Backplane Trigger C
1 0 0	Backplane Trigger D

Note: Refer to section 4.6 for details on synchronizing multiple cards.

Misc. Synchronization Control

29

Bit	7	6	5	4	3	2	1	0
Write	-	EOSOUT			-	-	-	-
Read	-	EOSOUT			-	-	-	-

EOSOUT ⇨ End of Sequence Output

0 0 0	None (default)
0 0 1	Backplane Trigger A
0 1 0	Backplane Trigger B
0 1 1	Backplane Trigger C
1 0 0	Backplane Trigger D

Note: Refer to section 4.6 for details on synchronizing multiple cards.

Figure 3. I/O Registers (continued)

Step Time MSB

2B Bit	7	6	5	4	3	2	1	0
Write	Step Time MSB (1µs/Bit)							
Read	Step Time MSB (1µs/Bit)							

Step Time LSB

2D Bit	7	6	5	4	3	2	1	0
Write	Step Time LSB (1µs/Bit)							
Read	Step Time LSB (1µs/Bit)							

Step Time (1µs/Bit) ⇨ The period of the internal step signal. This register is only used if the source of the step signal is set to Internal (Step Control Register (25_{16}) Bits 0-3 = 0_{16})

Note: Snapshots require a maximum amount of time to complete. Programming the step time less than or equal to this specified time will result in invalid snapshot measurements. Refer to the Pulse Period specification in section 1.2.2 for details.

Channel End

2F Bit	7	6	5	4	3	2	1	0
Write	End							
Read	End							

End ⇨ The last channel to be activated in the sequence.

Channel Start – 1

31 Bit	7	6	5	4	3	2	1	0
Write	Start – 1							
Read	Start – 1							

Start - 1 ⇨ The first channel (-1) to be activated in the sequence.

Figure 3. I/O Registers (continued)

Interrupt Enable MSB

Bit	7	6	5	4	3	2	1	0
Write	OCP	-	-	-	Ext2 Min	Ext2 Max	Ext1 Min	Ext1 Max
Read	OCP	-	-	-	Ext2 Min	Ext2 Max	Ext1 Min	Ext1 Max

Interrupt Enable LSB

3F

Bit	7	6	5	4	3	2	1	0
Write	Ilo Min	Ilo Max	Ihi Min	Ihi Max	Vlo Min	Vlo Max	Vhi Min	Vhi Max
Read	Ilo Min	Ilo Max	Ihi Min	Ihi Max	Vlo Min	Vlo Max	Vhi Min	Vhi Max

Vhi Max ⇨ Vhi Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Vhi Min ⇨ Vhi Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Vlo Max ⇨ Vlo Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Vlo Min ⇨ Vlo Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ihi Max ⇨ Ihi Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ihi Min ⇨ Ihi Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ilo Max ⇨ Ilo Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ilo Min ⇨ Ilo Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ext1 Max ⇨ Ext1 Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ext1 Min ⇨ Ext1 Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ext2 Max ⇨ Ext1 Maximum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
Ext2 Min ⇨ Ext1 Minimum Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)
OCP ⇨ Over Current Protect Interrupt Enable (0 = Interrupt disabled, 1= Interrupt enabled)

Note: The Master Interrupt Enable Bit (MIEN) in the Control/Status register (01_{16}) must be set for interrupt requests to be passed onto the m-module bus.

Vhi Maximum

41

Bit	7	6	5	4	3	2	1	0
Write	Vhi Max (816 mV/Bit)							
Read	Vhi Max (816 mV/Bit)							

Vhi Max ⇨ Maximum limit for the Vhi A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 816 mV/Bit. Refer to section 4.4 for details on setting limits.

Vhi Minimum

43

Bit	7	6	5	4	3	2	1	0
Write	Vhi Min (816 mV/Bit)							
Read	Vhi Min (816 mV/Bit)							

Vhi Min ⇨ Minimum limit for the Vhi A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 816 mV/Bit. Refer to section 4.4 for details on setting limits.

Figure 3. I/O Registers (continued)

Vlo Maximum

45 Bit	7	6	5	4	3	2	1	0
Write	Vlo Max (321 mV/Bit)							
Read	Vlo Max (321 mV/Bit)							

Vlo Max ⇨ Maximum limit for the Vlo A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 321 mV/Bit. Refer to section 4.4 for details on setting limits.

Vlo Minimum

47 Bit	7	6	5	4	3	2	1	0
Write	Vlo Min (321 mV/Bit)							
Read	Vlo Min (321 mV/Bit)							

Vlo Min ⇨ Minimum limit for the Vlo A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 321 mV/Bit. Refer to section 4.4 for details on setting limits.

Ihi Maximum

49 Bit	7	6	5	4	3	2	1	0
Write	Ihi Max (785 μA/Bit)							
Read	Ihi Max (785 μA/Bit)							

Ihi Max ⇨ Maximum limit for the Ihi A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 785 μA/Bit. Refer to section 4.4 for details on setting limits.

Ihi Minimum

4B Bit	7	6	5	4	3	2	1	0
Write	Ihi Min (785 μA/Bit)							
Read	Ihi Min (785 μA/Bit)							

Ihi Min ⇨ Minimum limit for the Ihi A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 785 μA/Bit. Refer to section 4.4 for details on setting limits.

Figure 3. I/O Registers (continued)

Ilo Maximum

4D Bit	7	6	5	4	3	2	1	0
Write	Ilo Max (785 μA/Bit)							
Read	Ilo Max (785 μA/Bit)							

Ilo Max ⇨ Maximum limit for the Ilo A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 785 μA/Bit. Refer to section 4.4 for details on setting limits.

Ilo Minimum

4F Bit	7	6	5	4	3	2	1	0
Write	Ilo Min (785 μA/Bit)							
Read	Ilo Min (785 μA/Bit)							

Ilo Min ⇨ Minimum limit for the Ilo A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is 785 μA/Bit. Refer to section 4.4 for details on setting limits.

Ext1 Maximum

51 Bit	7	6	5	4	3	2	1	0
Write	Ext1 Max							
Read	Ext1 Max							

Ext1 Max ⇨ Maximum limit for the Ext1 A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is determined by the external A/D logic. Refer to section 4.4 for details on setting limits.

Ext1 Minimum

53 Bit	7	6	5	4	3	2	1	0
Write	Ext1 Min							
Read	Ext1 Min							

Ext1 Min ⇨ Minimum limit for the Ext1 A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is determined by the external A/D logic. Refer to section 4.4 for details on setting limits.

Figure 3. I/O Registers (continued)

Ext2 Maximum

55 Bit	7	6	5	4	3	2	1	0
Write	Ext2 Max							
Read	Ext2 Max							

Ext2 Max ⇨ Maximum limit for the Ext2 A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is determined by the external A/D logic. Refer to section 4.4 for details on setting limits.

Ext2 Minimum

57 Bit	7	6	5	4	3	2	1	0
Write	Ext2 Min							
Read	Ext2 Min							

Ext2 Min ⇨ Minimum limit for the Ext2 A/D converter. When this limit is exceeded the corresponding bit in the interrupt pending register will be set. This value represents the upper 8-bits of the 12-bit value compared to the raw A/D data. The bit resolution is determined by the external A/D logic. Refer to section 4.4 for details on setting limits.

Interrupt Pending MSB

59 Bit	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-
Read	OCP	-	-	-	Ext2 Min	Ext2 Max	Ext1 Min	Ext1 Max

Interrupt Pending LSB

5B Bit	7	6	5	4	3	2	1	0
Write	(clear interrupts)							
Read	Ilo Min	Ilo Max	Ihi Min	Ihi Max	Vlo Min	Vlo Max	Vhi Min	Vhi Max

Vhi Max ⇨ Vhi Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Vhi Min ⇨ Vhi Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
Vlo Max ⇨ Vlo Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Vlo Min ⇨ Vlo Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
Ihi Max ⇨ Ihi Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Ihi Min ⇨ Ihi Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
Ilo Max ⇨ Ilo Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Ilo Min ⇨ Ilo Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
Ext1 Max ⇨ Ext1 Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Ext1 Min ⇨ Ext1 Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
Ext2 Max ⇨ Ext1 Maximum Interrupt Pending (0 = Not Pending, 1= Pending)
Ext2 Min ⇨ Ext1 Minimum Interrupt Pending (0 = Not Pending, 1= Pending)
OCP ⇨ Over Current Protect Interrupt Pending (0 = Not Pending, 1= Pending)

Note: A Write to address 5B will clear all interrupt pending bits except the Over Current Protection bit which can only be cleared by a reset.

Figure 3. I/O Registers (continued)

Channel Number -1

5D Bit	7	6	5	4	3	2	1	0
Write	(read only)							
Read	Channel Number -1							

Channel Number -1 ⇨ The channel (-1) that is currently being driven or, if idle, the last channel (-1) that was driven. During an over current condition a read of this register will return FE_{16}.

Revision

5F Bit	7	6	5	4	3	2	1	0
Write	(read only)							
Read	Revision							

Revision ⇨ The revision level of the on-board digital logic.

Figure 3. I/O Registers (continued)

4.0 PROGRAMMING INSTRUCTIONS

4.1 OVERVIEW

The MA201 is a register-based instrument that is controlled through a series of I/O registers described in section 3.4.1. The module only supports 8-bit reads and writes to I/O space. However, all registers are implemented using the odd bytes of the modules I/O space to facilitate 16-bit word addressing. If a 16-bit read or write is performed, the even byte is simply ignored by the module. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

Basic operation of the module involves setting up the channel sequence, configuring the step and snapshot timing signals, setting up A/D limits and interrupts, and starting the module. If enabled, interrupt requests will be generated and must be handled whenever a programmed limit is exceeded. Snapshot data is stored in memory at each step in the sequence. This data can be read through the I/O registers but only when the module is idle.

4.2 CONFIGURING AND RUNNING THE SEQUENCE

When the RUN bit in the Control/Status Register (01_{16}) is set, the MA201 will sequence from the programmed start channel to the programmed end channel at a rate determined by an internal step signal. At each step in the sequence an internal snapshot signal will trigger an acquisition and storage of data from all 6 A/D converters. The start and end channels are programmed through the Channel Start -1 Register (31_{16}) and the Channel End Register ($2F_{16}$).

The step signal can originate from an internal counter programmed through the Step Time Registers ($2B_{16}$ & $2D_{16}$), the software STEP bit in the Control/Status Register (01_{16}), or any of the four backplane trigger lines. The source of the step signal is selected by programming the Step Control Register (29_{16}). Refer to section 4.6 for details on using the trigger lines to control the step signal.

CAUTION:	The maximum voltage specifications are only valid when the sequence is running. When using a step select setting other than "Internal" verify that the step signal is running before providing a voltage higher than the constant level maximum specification.

The snapshot will occur at either a programmed time after the step signal or on the rising or falling edge of any of the four trigger lines. The source of the snapshot signal can be selected by programming the Snapshot Control Register (27_{16}). If the source of the snapshot signal is set to "Internal" then the value of the Snapshot Time Register ($0B_{16}$) will determine how long after the step signal a snapshot is taken. For details on using the trigger lines to control the snapshot signal refer to section 4.6.

4.3 READING SNAPSHOTS

A/D data is stored into memory in consecutive blocks of 13 bytes called snapshots. Each snapshot contains 2 bytes of data from all four on-board A/D converters, and from both external A/D interfaces. If the external A/D interfaces are not being used then their memory locations in the snapshot contain invalid data. The final byte of the snapshot is the 0-based channel number being driven at the time of the snapshot. Figure 4 shows the organization of a snapshot.

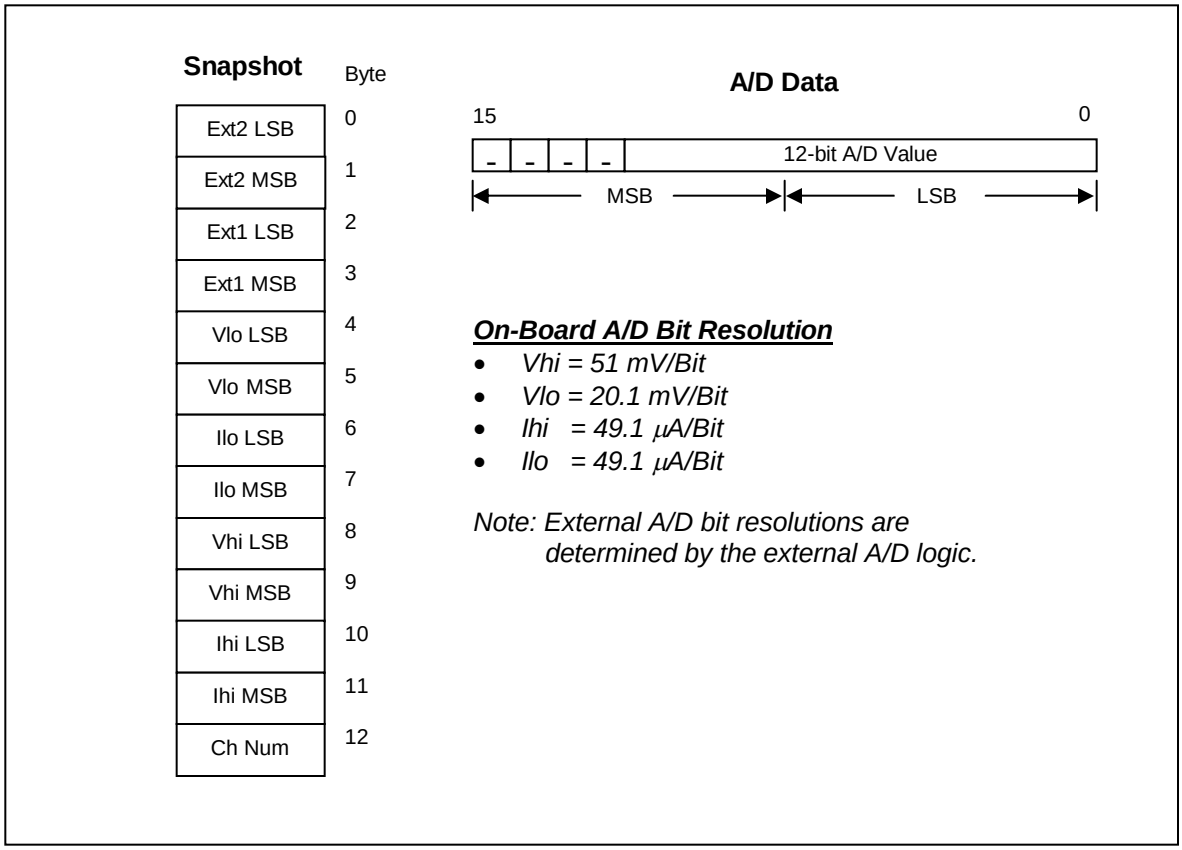


Figure 4. Snapshot Organization

The MA201 maintains two internal memory pointers both accessed through the Memory Address Registers (05_{16} & 07_{16}). The A/D Memory Pointer is a read only pointer that is accessed by reading the Memory Address Register. The pointer addresses the next memory location where the MA201 will store a snapshot. The User Memory Pointer is a write only pointer and is accessed by writing to the Memory Address Registers. This pointer addresses the next memory location from which a read of the Snapshot Data Register (03_{16}) will fetch data.

Snapshot data is read using the Snapshot Data Register (03_{16}) and the Memory Address Registers (05_{16} & 07_{16}) and can only be read when the MA201 is idle. The user must first read the A/D pointer and calculate the address of the first byte of a snapshot using the following formula:

$$UserMemoryPtr = A2DMemoryPtr - (NumDesiredSnapshots \times 13)$$

If this formula yields a negative result and the wrap bit in the Control/Status Register (01_{16}) is set then the pointer has wrapped around and 32,768 must be added to the calculated pointer. If the wrap bit is not set and the formula yields a negative result then total number of snapshots stored in memory is less than the number of desired snapshots.

Once the user memory pointer is calculated and written to the Memory Address Registers (05_{16} & 07_{16}) a read of the Snapshot Data Register will return the first byte of snapshot data. A read of the Snapshot Data Register will auto-increment the user memory pointer. Therefore each consecutive read of the Snapshot Data Register will return the next byte of the snapshot. Snapshots are stored consecutively in memory, therefore after all 13 bytes of a snapshot are read, the next read of the Snapshot Data Register will return the first byte of the next snapshot. The user should always treat the last snapshot stored as invalid since there is a high probability that the module was stopped while this snapshot was being taken yielding invalid results. Figure 5 diagrams the snapshot reading operation.

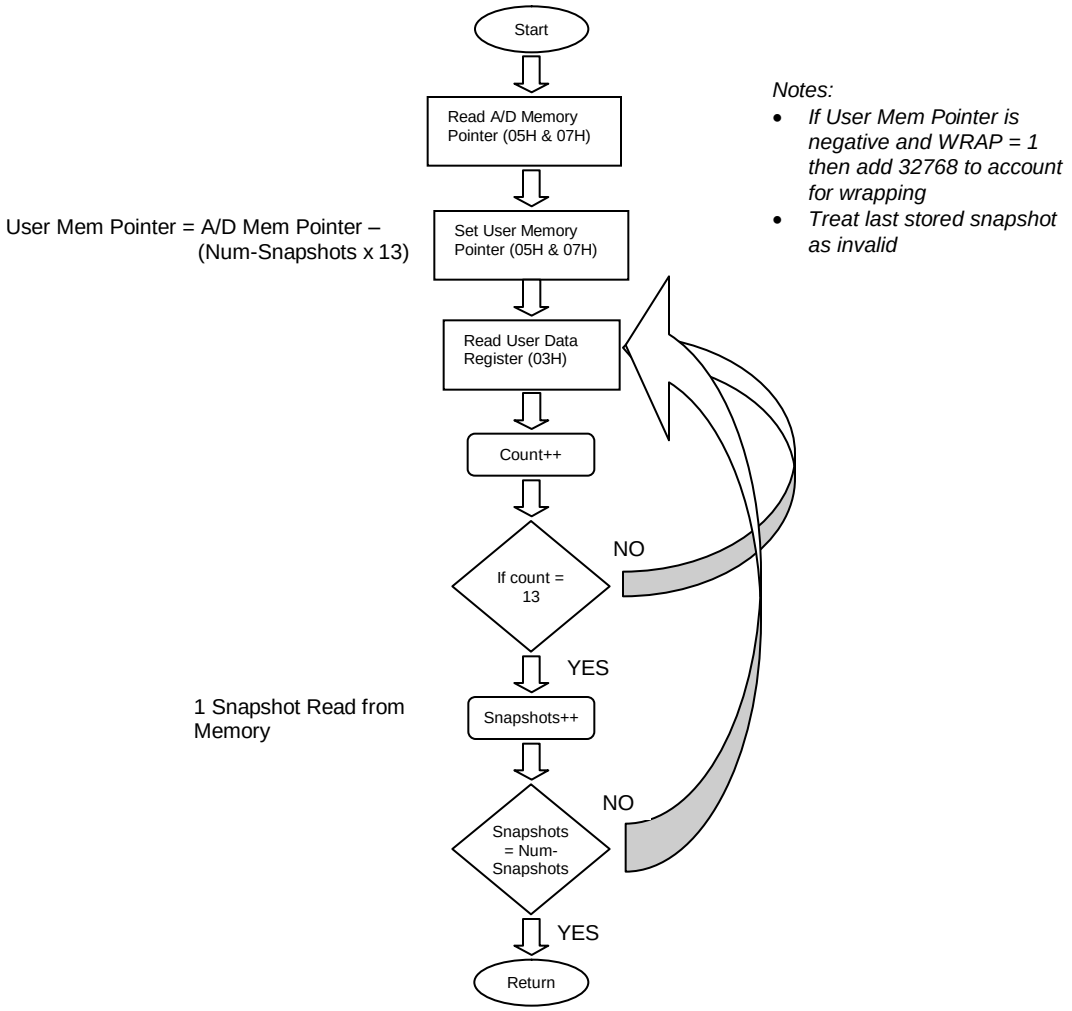


Figure 5. Snapshot Fetch Operation

4.4 LIMITS AND INTERRUPTS

The MA201 supports type A interrupts as specified by the M-module specification. A type A interrupt releases the interrupt request only after the pending interrupt is cleared by software (software-end-of-interrupt (i.e. RORA)).

For any interrupt to occur, the interrupt request line must be enabled by writing a one to the Master Interrupt Enable (MIEN) bit in the Control Status Register (01_{16}). Each type of interrupt can then be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Registers ($3D_{16}$ & $3F_{16}$).

The MA201 supports 13 different interrupts. A maximum and a minimum limit for each of the 6 A/D readings and an over current protection interrupt. The Interrupt Pending Registers (59_{16} & $5B_{16}$) contains 1 bit for each type of interrupt. If a bit is set to one then the corresponding limit has been exceeded. All interrupts are cleared by writing to the Interrupt Pending LSB Register ($5B_{16}$) except for the over-current protect interrupt which can only be cleared on a reset.

Vhi Maximum and Minimum: Limits for the high voltage rail readings. If the Vhi reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Vlo Maximum and Minimum: Limits for the low voltage rail readings. If the Vlo reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Ihi Maximum and Minimum: Limits for the high driver's current readings. If the Ihi reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Ilo Maximum and Minimum: Limits for the low drivers' current readings. If the Ilo reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Ext1 Maximum and Minimum: Limits for the external 1 A/D readings. If the Ext1 reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Ext2 Maximum and Minimum: Limits for the external 2 A/D readings. If the Ext2 reading exceeds these limits when a snapshot is taken an interrupt request will be generated.

Over Current Protect: If the current being drawn by either the high or low drivers exceed the over current protection limit then an interrupt request will be generated and all channels will be shut off. Over current protection logic monitors the current at all times, regardless of whether the module is running or not.

Limits are set for each A/D by programming the corresponding maximum and minimum register (41_{16} to 57_{16}). The values in these registers represent the upper 8-bits of a 12-bit value that is compared to the A/D readings each time a snapshot is taken. When we adjust the A/D bit resolution from Figure 4 to account for only 8-bits we get the bit resolutions values for the limit registers as follows:

- Vhi Maximum and Minimum: 816 mV/Bit
- Vlo Maximum and Minimum: 321 mV/Bit
- Ihi Maximum and Minimum: 785 μA/Bit
- Ilo Maximum and Minimum: 785 μA/Bit

Note: The bit resolutions for the external maximum and minimum limits registers are determined by the external A/D logic.

4.5 OVER CURRENT PROTECTION

The over current protection logic monitors the currents being drawn or sourced by all the low drivers and the high driver. If either of these currents exceed the over current protection threshold then an over current condition exists and all drivers will be shut off and the over current protect interrupt pending bit in the Interrupt Pending Register (59_{16}) will be set. If the over current protection interrupt is enabled then an interrupt request will be generated. Once an over current condition is met the drivers will remain off and an interrupt will remain pending until a one is written to the reset bit in the Control/Status Register (01_{16}).

Over current protection monitors the currents at all times except for during the programmable bypass period after a step in the sequence. The bypass time is programmable through the Bypass Register (09_{16}). Surge currents can exist when the drivers are changing states causing inherent over current conditions that the user may want to ignore. The bypass time should be programmed for a long enough period to ignore these currents.

4.6 SYNCHRONIZATION WITH OTHER MODULES

The four backplane triggers found on the MA201 allow the module to easily be synchronized with other instruments. The triggers can be programmed to initiate the two major functions of the MA201: stepping the sequence and taking a snapshot. Control of other instruments by the MA201 is also possible by programming the module to output, to the backplane triggers, its step signal, an end of sequence signal, and its snapshot signal.

The following two examples illustrate the basic synchronization capabilities of the MA201. They are intended to give the user a general understanding of the synchronization tools the MA201 employs.

4.6.1 Example 1: Cascading MA201's

In applications were more than 24 channels are required multiple MA204's can be cascaded as in this example. To perform this function each MA201 must know how many total channels are in the cascaded setup and where its first channel lies in the sequence.

For this example we will use two MA201's to sequentially drive 36 channels. Using the Total Num Channels +1 Register ($0D_{16}$) and the Sequence Register ($0F_{16}$) we can select where each card's channels lie in 36 channel sequence. To illustrate, both setups below provide 36 channels. In the first setup, channels 1-24 are Module A's channels 1-24 and channels 25-36 are Module B's channels 1-12. In the second setup, channels 1-12 are Module A's channels 1-12 and channels 25-36 are Module B's channels 0-24.

Setup 1	
Module A Total Num Channels +1 (Reg 0D) = 36 (24_{16}) Sequence (Reg 0F) = 1 Channel Start -1 (Reg 31) = 0 Channel End (Reg 2F) = 24	**Module B** Total Num Channels +1 (Reg 0D) = 36 (24_{16}) Sequence (Reg 0F) = 25 Channel Start -1 (Reg 31) = 0 Channel End (Reg 2F) = 12

Setup 2	
Module A Total Num Channels +1 (Reg 0D) = 36 (24_{16}) Sequence (Reg 0F) = 1 Channel Start -1 (Reg 31) = 0 Channel End (Reg 2F) = 12	**Module B** Total Num Channels +1 (Reg 0D) = 36 (24_{16}) Sequence (Reg 0F) = 13 Channel Start -1 (Reg 31) = 0 Channel End (Reg 2F) = 24

For further synchronization one module can provide its step and snapshot signals to the other via the backplane trigger lines. This way the entire sequence runs off the same step signal and snapshots on both cards happen at the same time. For this example, Module A will provide its step signal to Module B via trigger A and its snapshot signal via Trigger B. Both signals will be produced from the internal counters of Module A.

Module A Synch Control (Reg 25) = 12_{16} (Step Out = TrigA, Snapshot Out = TrigB) Synch Control (Reg 27) = 00_{16} (Snapshot = Internal) Synch Control (Reg 29) = 00_{16} (StepSel = Internal)	**Module B** Synch Control (Reg 25) = 00_{16} (Step Out = None, Snapshot Out = None) Synch Control (Reg 27) = 04_{16} (Snapshot = Trig B (rising)) Synch Control (Reg 29) = 02_{16} (StepSel = Trig A (rising))

4.6.2 Example 2: Row Column Matrix Setup

For applications such as display testing, a matrix setup might be desired to sequence through rows and columns. Using two MA201's, one as a row driver and one as a column driver, a 24x24 channel matrix can be achieved. Larger matrices can be configured by cascading MA201's as in example 1 above. For this example we will setup a 10x12 (row x column) matrix. Every point in the matrix will be driven for the same amount of time and at each point a snapshot will be taken from both cards.

In the setup below Module A is the row driver and Module B is the column driver. Module B will use its internal primary timer for its step signal. It will also use its internal snapshot timer for its snapshot signal. Module A will use the End of Sequence originating from Module B via Trigger A as its step signal. Module A will also use Module B's snapshot signal via Trigger B.

Module A	**Module B**
Total Num Channels + 1 (Reg 0D) = 11 ($0B_{16}$)	Total Num Channels +1 (Reg 0D) = 13 ($0D_{16}$)
Sequence (Reg 0F) = 1	Sequence (Reg 0F) = 1
Channel Start -1 (Reg 31) = 0	Channel Start -1 (Reg 31) = 0
Channel End (Reg 2F) = 10 ($0A_{16}$)	Channel End (Reg 2F) = 12 ($0C_{16}$)
Synch Control (Reg 25) = 00_{16} (Step Out = None, Snapshot Out = None)	Synch Control (Reg 25) = 02_{16} (Step Out = None, Snapshot Out = Trig B)
Synch Control (Reg 27) = 04_{16} (Snapshot = Trig B (rising))	Synch Control (Reg 27) = 00_{16} (Snapshot = Internal)
Synch Control (Reg 29) = 02_{16} (StepSel = Trig A (rising))	Synch Control (Reg 29) = 10_{16} (EOSOut = Trig A, StepSel = Internal)

APPENDIX A – CONNECTORS

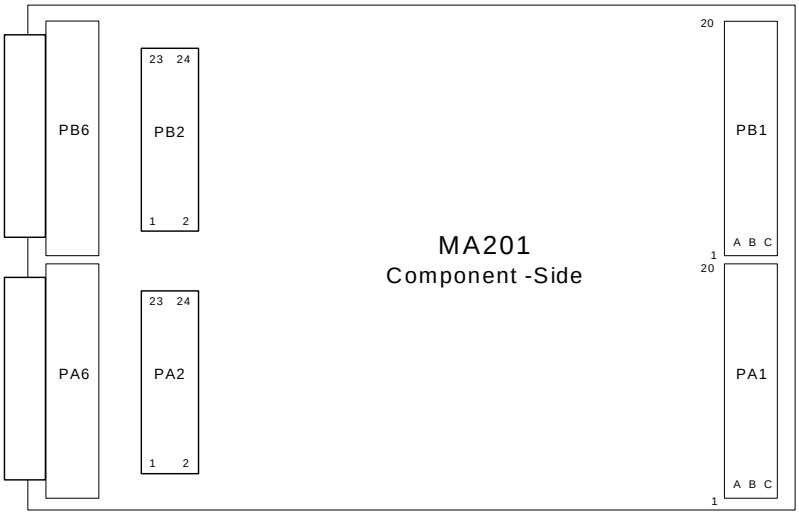


Figure A-1. Connector Orientation

PA1

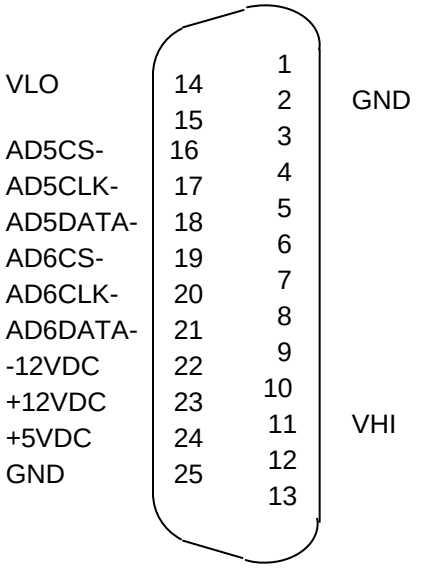
Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	(D16)
3	A02	+12V	(D17)
4	A03	-12V	(D18)
5	A04	GND	(D19)
6	A05	(/DREQ)	(D20)
7	A06	(/DACK)	(D21)
8	A07	GND	(D22)
9	(D08)	D00/(A08)	TRIGA
10	(D09)	D01/(A09)	TRIGB
11	(D10)	D02/(A10)	(D23)
12	(D11)	D03/(A11)	(D24)
13	(D12)	D04/(A12)	(D25)
14	(D13)	D05/(A13)	(D26)
15	(D14)	D06/(A14)	(D27)
16	(D15)	D07/(A15)	(D28)
17	(/DS1)	/DS0	(D29)
18	DTACK	/WRITE	(D30)
19	/IACK	/IRQ	(D31)
20	/RESET	SYSCLK	(/DS2)

Note: Signals in parentheses ( ) are not used on this module.

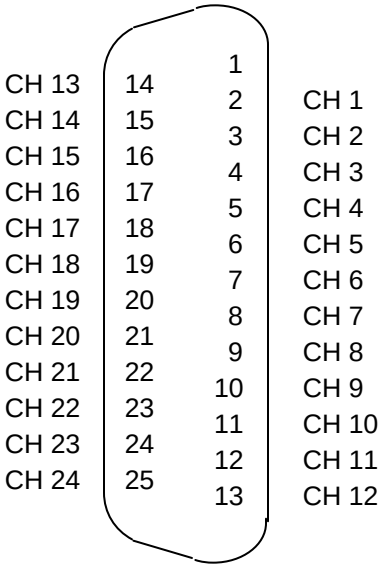
Figure A-2. M/MA Connector Configuration (PA1)

PB1			
Pin	Row A	Row B	Row C
1	-	-	-
2	-	-	-
3	-	+12V	-
4	-	-12V	-
5	-	-	-
6	-	-	-
7	-	-	-
8	-	-	-
9	-	-	TRIGC
10	-	-	TRIGD
11	-	-	-
12	-	-	-
13	-	-	-
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-

Figure A-2. M/MA Connector Configuration (PB1)



PB6



PA6

Figure A-3. Front Panel D-Sub Connector Configurations (PA6 & PB6)

PA2			
PIN	SIGNAL	PIN	SIGNAL
1	CH12	2	CH24
3	CH11	4	CH23
5	CH10	6	CH22
7	CH9	8	CH21
9	CH8	10	CH20
11	CH7	12	CH19
13	CH6	14	CH18
15	CH5	16	CH17
17	CH4	18	CH16
19	CH3	20	CH15
21	CH2	22	CH14
23	CH1	24	CH13

PB2			
PIN	SIGNAL	PIN	SIGNAL
1	-	2	GND
3	-	4	+5V
5	VHI	6	+12V
7	-	8	-12V
9	-	10	AD6DATA-
11	-	12	AD6CLK-
13	-	14	AD6CS-
15	-	16	AD5DATA-
17	-	18	AD5CLK-
19	-	20	AD5CS-
21	-	22	-
23	GND	24	VLO

Figure A-4. Peripheral Connector Configurations (PA2 & PB2)

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