U S E R ' S M A N U A L

3-CHANNEL CLOCK/ COUNTER/ TIMER M-MODULE

MODEL M227

Document Part No: 11030384

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NOTE

The contents of any amendment may affect operation, maintenance, or calibration of the equipment.

INTRODUCTION

This manual describes the operation and use of the C&H Model M227 3-Channel Clock/Counter/Timer (Part Number 11030380). This module is designed to interface with any standard M-Module carrier.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The M227 module provides a variety of clock, counter, and timer functions, including a number of derived counter outputs and three 32-bit counters.

The module conforms to the ANSI/VITA 12-1996 standard for M-modules, which allows it to be used in a variety of platforms, including VXI, LXI, PXI, VME, PCI, cPCI, and Ethernet, with the use of an M-module carrier.

1.1 PURPOSE OF EQUIPMENT

This instrument is designed for precise clocking, counting, and timing applications required in data acquisition and test applications. The instrument can provide precise triggering signals to data acquisition equipment, produce a variety of pulse stimuli, and perform pulse count and time period measurement functions.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- On-board 50 MHz oscillator
- Three Pre-loadable 32-bit Up/Down Counters with Programmable Match Functions
- Two Programmable 32-bit Dividers
- Flexible Asynchronous or Synchronous Gating/Trigger Functions
- On-the-fly Synchronous Latching of 32-bit Count Values
- Easily Perform Pulse Width, Period, and Interval Measurements
- Programmable Outputs
- Interrupt and M-Trigger Support
- On-board oscillator can be disciplined to an external signal to provide increased accuracy and long term stability

1.2.2 Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Operating Temperature		0 to +50	°C
Non-Operating Temperature		-40 to +71	°C
Humidity	non-condensing	5 to 95	%
Power Consumption	+5V	80 (typ), 100 (max)	mA
	+12V	5 (typ), 10 (max)	mA
	-12V	12 (typ), 15 (max)	mA
Input Voltage (all inputs)	no damage, power off	± 40	V
	no damage, power on	± 36	V

SPECIFICATIONS (full operating temperature, unless otherwise specified)

Parameter	Conditions	Min	Typ.	Max	Units
Derived Outputs					
Driver Type	Two 74ABT125 outputs in parallel with a 25Ω series resistor				
Output High Voltage	V_{OH} at -6ma	2.5			V
	V_{OH} at -64ma	2.0			V
Output Low Voltage	V_{OL} at 128ma			0.55	V
Counters					
Frequency				50	MHz
Inputs (FPINA/B)					
Threshold Level	LVLx = 0 [2]		1.4		V
	LVLx = 1		0.8		V
Input Impedance	IMPx = 0 [2]	900K	1M		Ω
	IMPx = 1		50		Ω
On-board Oscillator					
Frequency				50	MHz
Stability				±50	ppm

Notes:
1. The stability can be improved by disciplining the internal clock to an external reference clock. The internal clock accuracy will discipline in about 10 minutes to within one decade of the external reference, up to 10^{-8} accuracy.
2. For LVLx and IMPx refer to register bits in the *Input/Output Control* register. Refer to Figure 4.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (106.2 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	M-Module
Addressing:	A08
Data:	D16
Interrupts:	INTB (ROAK)
DMA:	not supported
Triggers:	MTRGA & MTRGB
Identification:	IDENT and VXI-IDENT
Manufacturer ID:	$0FC1_{16}$
Model Number:	$00E3_{16}$ (227 dec.)
VXI Model Code:	$0FD6_{16}$ (M227)

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The M227 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M-Module and carrier.

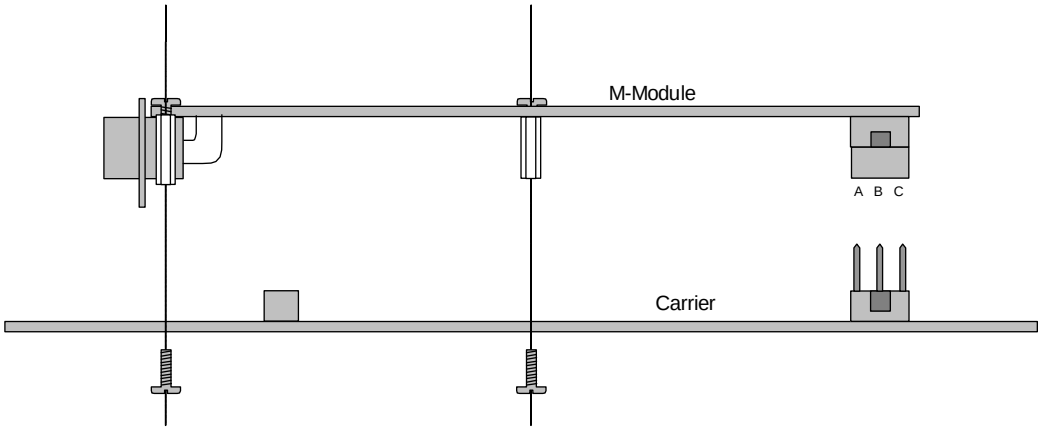

Figure 1. M-Module Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

A simplified functional block diagram of the module is shown in Figure 2.

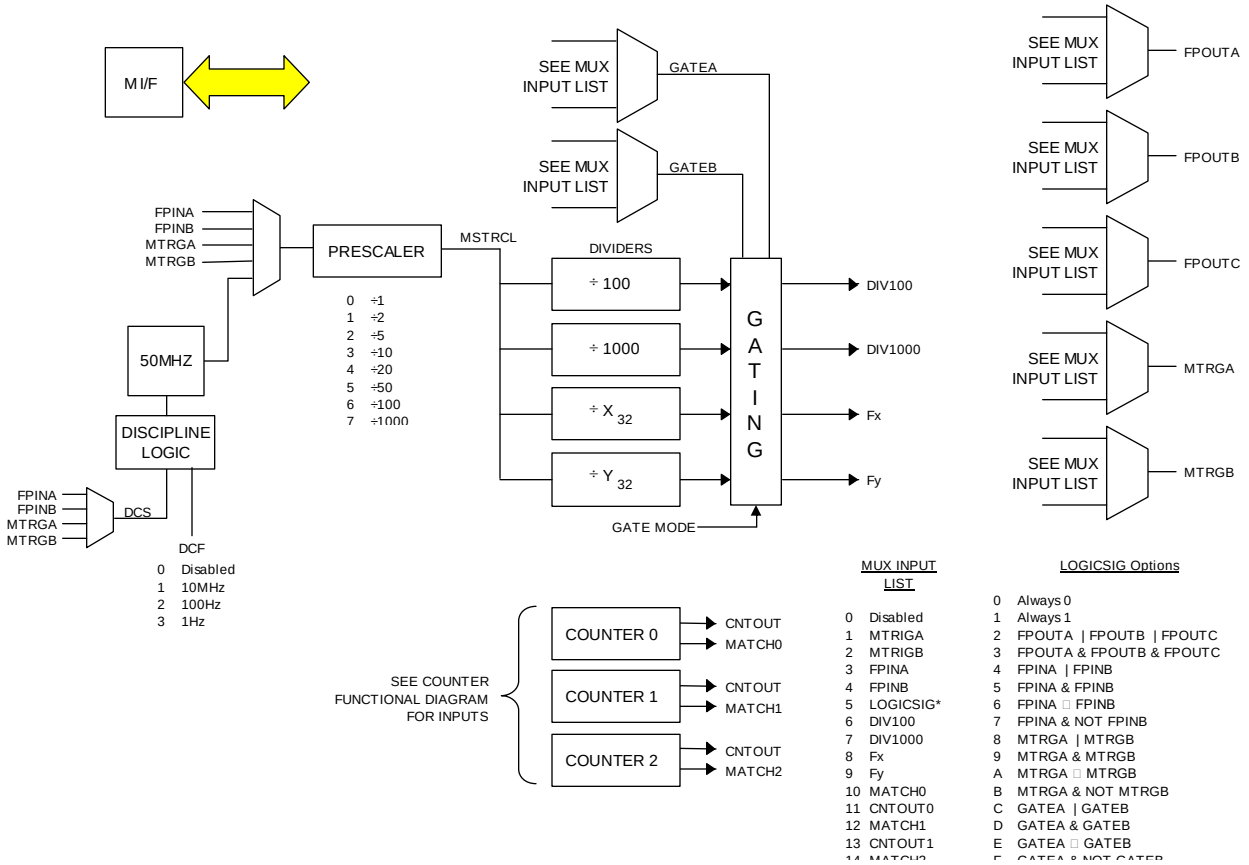

Figure 2. Functional Block Diagram

3.1.1 Dividers

Four 32-bit modulo-N dividers derive four different counters from the Master Clock. These counters are available at the front panel, bus trigger lines, and at the inputs of the counters. Two are fixed to divide the Master Clock by 100 and 1000 and the other two are programmable (Fx and Fy).

3.1.2 Gating

The gating function provides asynchronous or synchronous gating of the four derived signals. The derived signals can be enabled/disabled by software or various internal or external signals or combination of signals. The external gating signal can be mapped to any of the bus trigger lines, the derived counters, and other signals.

3.1.3 Discipline Logic

The on-board 50MHz oscillator can be disciplined to an external source to obtain better accuracy and long term stability. The external signal frequency can be 10MHz, 100Hz, or 1Hz (1PPS).

3.1.4 Prescaler

The Master Clock can be prescaled by 2, 5, 10, 20, 50, 100, or 1000 before it is used internally.

3.1.5 LOGICSIG Options

The LOGICSIG provides special logical operations to be applied to various signals. These AND, OR, Exclusive OR, and NOT functions allow signals to be combined "logically" before use or output.

3.1.6 Counters

There are three 32-bit binary counters available for general counting/timing functions as shown in Figure 3. The clock, reset, enable, and latch inputs to each counter can be selected from the Master Clock, any of the derived frequencies, the M-Module trigger lines, the front panel trigger input, or the output of another counter. The counters can count up or down and can either free run or stop on carry/borrow. The carry/borrow output of each counter is programmable as a square wave or a pulse. An interrupt can be generated upon carry/borrow, when the count value equals a match register value, or when the count value is latched. The 32-bit count value can be read on-the-fly or it can be latched upon a signal event for event time measurement applications.

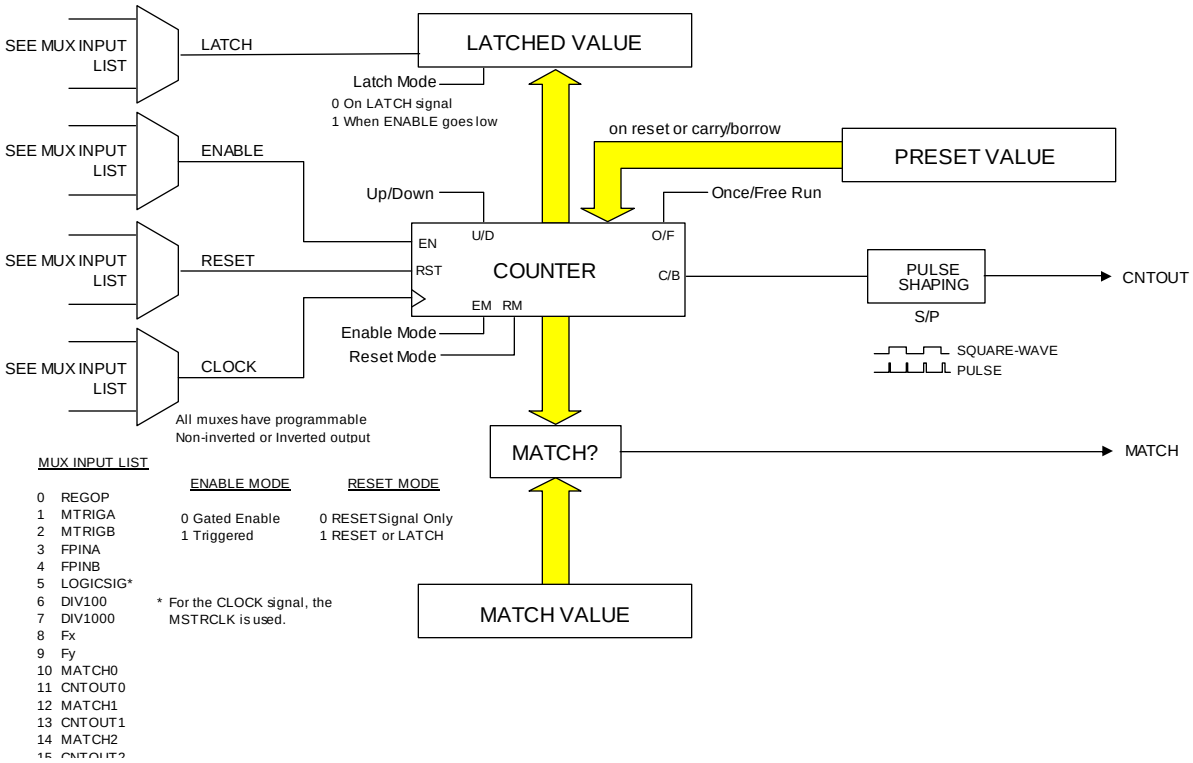

Figure 3. Counter Functional Diagram

3.2 INPUT/OUTPUT SIGNALS

The front panel I/O connector is a 5-pin 5W5S D-Sub Socket connector with 50Ω coaxial contacts (FCT Housing P/N FM5W5S-K121 and FCT Contact P/N FME008S102 or equivalent). Below are the signals and functional descriptions provided on the connector (see Appendix A for pin assignments).

FPINA/B These contacts can be used to input external triggering, gating, and clocking stimulus. There use is fully software programmable. The input impedance is programmable for >10KΩ or 50Ω and the input threshold is programmable as 0.8V or 1.4V.

FPOUTA/B/C These contacts can be programmed to output any of the derived gated signals, any of the counter outputs, or either of the M-Module triggers. The outputs have a 50Ω output impedance.

3.3 CONFIGURATION AND IDENTIFICATION

3.3.1 Programming Registers

There are a variety of registers used to configure and control the M227 module. These registers are located as offset from the base address of the module. The absolute address depends on the M-module carrier for which the M227 is installed. See the carrier's User Manual for details. The address map of the registers is shown in Table I. Details of the registers are provided in Figure 4.

Table I. Address Map

IO REG. (HEX)	REGISTER DESCRIPTION
00	ID
02	Revision
04	Master Control
06	Interrupt Control
08	Interrupt Status
0A	Gate Control
0C	Input/Output Control
0E	Input Status
10	Logic/Output Source Map
12	Gate/M-Trigger Source Map Register
14-1E	(reserved)
20/30/40	Counter X Control
22/32/42	Counter X Input Source Map
24/34/44	Counter X Preset Value (High)
26/36/46	Counter X Preset Value (Low)
28/38/48	Counter X Latch Value (High)
2A/3A/4A	Counter X Latch Value (Low)
2C/3C/4C	Counter X Match Value (High)
2E/3E/4E	Counter X Match Value (Low)
50	Fx Divider Value (High)
52	Fx Divider Value (Low)
54	Fy Divider Value (High)
56	Fy Divider Value (Low)
FE	IDPROM

Reg 00

ID Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read only)								(read only)							
Read	Configuration								Model							

Configuration ⇨ Configuration Number (dash number of the unit according to the following table)
0 Normal
Others Undefined
Model ⇨ Model Number (always reads hex E3, decimal 227)

Reg 02

Revision Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	(read only)								(read only)							
Read	FWMAJ				FWMIN				HWMAJ				HWMIN			

FWMAJ ⇨ Firmware Major Revision (first major release is 1, prerelease is 0)
FWMIN ⇨ Firmware Minor Revision (minor releases involve insignificant changes or corrections)
HWMAJ ⇨ Hardware Major Revision (first major release is 1, prototype is 0)
HWMIN ⇨ Hardware Minor Revision (minor releases involve insignificant changes or corrections)

Reg 04

Master Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	RFSRC			-	-	RFMD		-	MCPS			-	MCS		
Read	0	RFSRC			RFDC	RFDT	RFMD		0	MCPS			0	MCS		

RFSRC ⇨ Reference Clock Source

0	Disabled (leave undisciplined)	4	MTRGB
1	FPINA	5	(reserved)
2	FPINB	6	(reserved)
3	MTRGA	7	(reserved)

RFDC ⇨ Internal Clock Disciplined (1 = internal clock is disciplined within range)
RFDT ⇨ External Reference Clock Detected (1 = an external reference clock has been detected)
RFMD ⇨ Reference Clock Mode/Frequency

0	1pps
1	100pps
2	1000Hz
3	10MHz

MCPS ⇨ Master Clock Pre-Scaler

0	÷1	4	÷20
1	÷2	5	÷50
2	÷5	6	÷100
3	÷10	7	÷1000

MCS ⇨ Master Clock Source

0	Internal 50MHz	4	FPINA
1	(reserved)	5	FPINB
2	(reserved)	6	MTRGA
3	(reserved)	7	MTRGB

Figure 4. Programming Registers

Reg 06

Interrupt Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	GIE	-	-	-	-	CIE2	MIE2	LIE2	-	CIE1	MIE1	LIE1	-	CIE0	MIE0	LIE0
Read	GIE	0	0	0	0	CIE2	MIE2	LIE2	0	CIE1	MIE1	LIE1	0	CIE0	MIE0	LIE0

GIE ⇨ Global Interrupt Enable (1 = enable)
CIEx ⇨ Carry/Borrow Interrupt Enable [1] (1 = enable)
MIEx ⇨ Match Interrupt Enable (1 = enable)
LIEx ⇨ Latch Interrupt Enable (1 = enable)

Note: GIE bit is automatically cleared when an interrupt acknowledge is issued. Software must re-enable interrupts to receive further interrupts.

Reg 08

Interrupt Status Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	CIP2	MIP2	LIP2	-	CIP1	MIP1	LIP1	-	CIP0	MIP0	LIP0
Read	0	0	0	0	0	CIP2	MIP2	LIP2	0	CIP1	MIP1	LIP1	0	CIP0	MIP0	LIP0

CIPx ⇨ Carry/Borrow Pending (1 = pending, writing a 1 clears pending interrupt)
MIPx ⇨ Match Interrupt Pending (1 = pending, writing a 1 clears pending interrupt)
LIPx ⇨ Latch Interrupt Pending (1 = pending, writing a 1 clears pending interrupt)

Figure 4. Programming Registers (continued)

Reg 0A

Gate Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	FyAG	FyGM			FxAG	FxGM			D3AG	DIV1000GM			D2AG	DIV100GM		
Read	FyAG	FyGM			FxAG	FxGM			D3AG	DIV1000GM			D2AG	DIV100GM		

xxAG ⇨ Asynchronous Gating for each of the clock signals (0 = synchronous, 1 = asynchronous)
xxGM ⇨ Mode of gating for each of the clock signals

- 000 (0) - Disabled
- 001 (1) - GATEA High enables
- 010 (2) - GATEA Low enables
- 011 (3) - GATEA ↑ enables, GATEB ↓ disables
- 100 (4) - GATEA ↓ enables, GATEB ↑ disables
- 101 (5) - GATEA ↑ enables, GATEB ↑ disables
- 110 (6) - GATEA ↓ enables, GATEB ↓ disables
- 111 (7) - Always Enabled

Reg 0C

Output Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	SPOC	SPOB	SPOA	SPTB	SPTA	-	-	IMOB	IMOA	-	IOC	IOB	IOA
Read	0	0	0	SPOC	SPOB	SPOA	SPTB	SPTA	0	0	IMOB	IMOA	0	IOC	IOB	IOA

IMOx ⇨ Invert MTRGA/B Output (0 = normal, 1 = invert)
IOx⇨Invert FPOUTA/B/C (0 = normal, 1 = invert)
SPOx ⇨ Square-Pulse Mode (outputs)
SPTx ⇨ Square-Pulse Mode MTrig (output)

Reg 0E

Input Status / Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	IMPB	IMPA	LVLB	LVLA	-	-	-	-	IMIB	IMIA	IIB	IIA	-	-	-	-
Read	IMPB	IMPA	LVLB	LVLA	0	0	0	0	IMIB	IMIA	IIB	IIA	STMB	STMA	STIB	STIA

STIA/B ⇨ Status of Front Panel Input Signals A & B (0 = low, 1 = high)
STMA/B ⇨ Status of Backplane MTRG Signals A & B (0 = low, 1 = high)
IMIx⇨Invert MTRGA/B Input (0 = normal, 1 = invert)
IIx⇨Invert FPINA/B (0 = normal, 1 = invert)

IMPA/B ⇨Input Impedance of Front Panel Inputs FPINA/B (0 = >10KΩ, 1 = 50Ω)
LVLA/B ⇨ Threshold Level of Front Panel Inputs FPINA/B (0 = 0.8V, 1 = 1.4V)

Note: The inversion of an input signal is applied immediately upon input and the inversion of an output signal is applied at the output of the source of the signal. Therefore, the internal logic always uses the inverted signal. For example, if FPINA is inverted (IIA = 1), then the inverted FPINA is used throughout the remaining logic. If FPOUTA is inverted (IOA = 1), then the inverted FPOUTA is used throughout the remaining logic.

Figure 4. Programming Registers (continued)

Reg 10

Logic/Output Source Map Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	LOGICSIG				OUTC				OUTB				OUTA			
Read	LOGICSIG				OUTC				OUTB				OUTA			

LOGICSIG ⇨ Logic Signal Sources and Logical Operation

0	Always 0	8	MTRGA | MTRGB
1	Always 1	9	MTRGA & MTRGB
2	FPOUTA | FPOUTB | FPOUTC	A	MTRGA ⊗ MTRGB
3	FPOUTA & FPOUTB & FPOUTC	B	MTRGA & NOT MTRGB
4	FPINA | FPINB	C	GATEA | GATEB
5	FPINA & FPINB	D	GATEA & GATEB
6	FPINA ⊗ FPINB	E	GATEA ⊗ GATEB
7	FPINA & NOT FPINB	F	GATEA & NOT GATEB

OUTx ⇨ Front Panel Output Source [1]

0	Disable	8	Fx (gated)
1	MTRGA (must be an input)	9	Fy (gated)
2	MTRGB (must be an input)	A	MATCH0
3	FPINA	B	CNTOUT0
4	FPINB	C	MATCH1
5	LOGICSIG	D	CNTOUT1
6	DIV100 (gated)	E	MATCH2
7	DIV1000 (gated)	F	CNTOUT2

Notes:

1. The Output Source can be set equal to the Master Clock by using the Fx or Fy signal with a divide value of 1.

Reg 12

Gate/M-Trigger Source Map Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	GATEA				GATEB				MTRGB				MTRGA			
Read	GATEA				GATEB				MTRGB				MTRGA			

GATEx ⇨ Gate Signal Source
MTRGx ⇨ M-Module Trigger Source

0	Disable/Input [1]	8	Fx (gated)
1	MTRGA (must be an input)	9	Fy (gated)
2	MTRGB (must be an input)	A	MATCH0
3	FPINA	B	CNTOUT0
4	FPINB	C	MATCH1
5	LOGICSIG	D	CNTOUT1
6	DIV100 (gated)	E	MATCH2
7	DIV1000 (gated)	F	CNTOUT2

Notes:

1. Setting the MTRG source to anything except 0, causes MTRGA/B to be enabled as an output.

Figure 4. Programming Registers (continued)

Counter X Control Register

Reg 20
30
40

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	IL	IE	IR	IC	LS	ES	RS	CS	LM	EM	RM	MM	S/P	O/F	U/D	ME
Read	IL	IE	IR	IC	LS	ES	RS	CS	LM	EM	RM	MM	S/P	O/F	U/D	ME

IL ⇨ Invert Latch Signal (1 = invert)
IE ⇨ Invert Enable Signal (1 = invert)
IR ⇨ Invert Reset Signal (1 = invert)
IC ⇨ Invert Clock Signal (1 = invert)
LS ⇨ Latch Signal (this level is presented to the Latch Mux and is used in register op mode)
ES ⇨ Enable Signal (this level is presented to the Enable Mux and is used in register op mode)
RS ⇨ Reset Signal (this level is presented to the Reset Mux and is used in register op mode)
CS ⇨ Clock Signal (this level is presented to the Clock Mux and is used in register op mode)
LM ⇨ Latch Mode (0 = latch on LATCH signal, 1 = latch when ENABLE goes low)
EM ⇨ Enable Mode (0 = gated, 1 = triggered)
RM ⇨ Reset Mode (0 = reset on RESET signal only, 1 = on RESET signal or automatically after latching)
MM ⇨ Master Mode (0 = normal, 1 = disable after latching) [1]
S/P ⇨ Square Wave/Pulse Select (0 = square wave, 1 = pulse) [2]
O/F ⇨ Once-through/Free Run Select (0 = once-through, 1 = Free run)
U/D ⇨ Up/Down Select (0 = count down, 1 = count up)
ME ⇨ Master Enable (0 = disabled, 1 = enabled)

Notes:
1. When MM = 1, the Master Enable (ME) bit is cleared when the LATCH signal occurs. When MM = 0, the ME bit is controlled entirely by software.
2. Use pulse mode when using the counter for counting functions.

Counter X Input Source Map Register

Reg 22
32
42

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	LSS				ESS				RSS				CSS			
Read	LSS				ESS				RSS				CSS			

LSS ⇨ Latch Signal Source
ESS ⇨ Enable Signal Source
RSS ⇨ Reset Signal Source
CSS ⇨ Clock Signal Source

0	Register Operation	8	Fx_GATED
1	MTRIGA	9	Fy_GATED
2	MTRIGB	A	MATCH0
3	FPINA	B	CNTOUT0
4	FPINB	C	MATCH1
5	MSTRCLK/LOGICSIG [1]	D	CNTOUT1
6	DIV100 (Gated)	E	MATCH2
7	DIV1000_GATED	F	CNTOUT2

Notes:
1. When defining the source for the Clock signal, a value of 5 sets the source to the Master Clock. For the Latch, Enable, and Reset signals, a value of 5 sets the source to the LOGICSIG.

Figure 4. Programming Registers (continued)

Counter X Preset Value (High) Register

Reg 24
34
44

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

Counter X Preset Value (Low) Register

Reg 26
36
46

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D31-D0 ⇨ Counter Preset Value (The value is only changed when the High register is written)

Counter X Latch Value (High) Register

Reg 28
38
48

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-Only								Read-Only							
Read	D31-D24								D23-D16							

Counter X Latch Value (Low) Register

Reg 2A
3A
4A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-Only								Read-Only							
Read	D15-D8								D7-D0							

D31-D0 ⇨ Counter Latch Value (The value is latched when LATCH signal occurs)

Note: To guarantee consistency between the High and Low registers, the High registers must be read first. Internally, the Low register is buffered when the High register is read.

Counter X Match Value (High) Register

Reg 2C
3C
4C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

Counter X Match Value (Low) Register

Reg 2E
3E
4E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D31-D0 ⇨ Counter Match Value (The value is only changed when the High register is written)

Figure 4. Programming Registers (continued)

Reg 50

Fx Divider Value (High) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

Reg 52

Fx Divider Value (Low) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D31-D0 ⇨ Fx Divide Value (The value is only changed when the High register is written)

Reg 54

Fy Divider Value (High) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D31-D24								D23-D16							
Read	D31-D24								D23-D16							

Reg 56

Fy Divider Value (Low) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15-D8								D7-D0							
Read	D15-D8								D7-D0							

D31-D0 ⇨ Fy Divide Value (The value is only changed when the High register is written)

Reg. FE

IDPROM Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used													CS	CLK	DIO
Read	0													CS	CLK	DIO

CS ⇨ IDPROM Chip Select
CLK ⇨ IDPROM Clock
DIO ⇨ IDPROM Data Input/Output

Note: See 3.3.2 for details on using this register.

Figure 4. Programming Registers (continued)

3.3.2 M-Module Identification PROM

The M227 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial EEPROM. Access is accomplished with read/write operations on the last address in IOSpace (0xFE) and the data is read one bit at a time. Instructions for reading the IDENT PROM are given in section 4.3.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the EEPROM to at least 64 words (128 bytes) and includes VXI compatible ID and Device Type Registers. Details are shown in Table II.

Table II. M-Module EEPROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	00E3 (227 dec.)
2	Revision Number [1]	1010
3	Module Characteristics [2]	1E48
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FC1 (C&H)
18	VXI Device Type [3]	FFD6
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) The Revision Number is the firmware and hardware functional revision level of the module. The hardware revision number does not necessarily correspond to the hardware assembly level. The bits definitions are:

Bit(s)	Description
15-12	Software Major Revision (1.0 is first major release)
11-8	Software Minor Revision
7-4	Hardware Major Revision (1.0 is first major release)
3-0	Hardware Minor Revision

2) The Module Characteristics bit definitions are:

Bit(s)	Description	Bit(s)	Description
15	0 = no burst access	8/7	00 = no DMA requestor
14/13	Unused	6/5	10 = INTB (INTA also supported)
12	1 = module needs ±12V	4/3	01 = 16-bit data
11	1 = module needs +5V	2/1	00 = 8-bit address bus
10	1 = trigger outputs supported	0	0 = no memory access
9	1 = trigger inputs supported		

3) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$FD6_{16}$ = C&H specified VXI model code for M227

4.0 OPERATION

The M227 is a register-based instrument that is controlled through a series of registers described in Section 3.3.1.

4.1 PROGRAMMING

The module is programmed through a series of accesses to the configuration registers. A high-level software driver may be available to aid in programming of the module.

4.2 COUNTERS

Each counter has a Control Register that is used to configure the various modes of the counter, such as up/down counting, input signal inversion, enable/reset/latching modes, and square or pulse output. There are also registers for the Preset Value (the value loaded upon reset or roll-over), the Match Value (the compare value used for MATCH signal generation), and a read-only register for the on-the-fly Latch Value. Each counter outputs a CNTOUT signal when it rolls over and a MATCH signal when the counter value equals the MATCH value.

In addition, each counter has four input signals that clock, reset, or enable the counter or latch the counter value. The input source of the CLOCK, RESET, ENABLE, and LATCH signals is software programmable to be a register operation, either of the M-Module Trigger signals, either front panel input signal, the Master Clock, any of the four derived gated clocks, any counter's match signal, or any counter's carry/borrow (CNTOUT) signal. This highly flexible architecture allows a variety of timing, counting, measurement, and pulsing operations.

4.2.1 Counting Functions

For general pulse counting functions, the counter should be configured in the count up mode and a preset value of zero. Depending on the application, the counter can be configured to stop on carry (once-through mode) or continuing counting after a roll-over (free run mode). The count value can be monitored using the Count Latch register. The Match Value register can be set and an interrupt generated when the Match Value is reached. The counter's input sources are controlled using the Counter Input Source Map register. The CLOCK source would be set to the signal that needs to be counted. The LATCH, ENABLE, and RESET source would be set to "Register Operation". The LS, ES, and RS bits in the Clock Control Register are then used to reset, enable, and latch the counter when desired.

4.2.2 Event Time Measurement

The M227 can be used to measure pulse width, period, and intervals between two signals. For instance, to measure the pulse width of FPINA, Counter 0 can be configured to ENABLE when FPINA is high. By setting the Latch Mode to Latch when ENABLE goes low, the pulse width can be easily determined. With the CLOCK input set to the Master Clock and a prescaler of 1, the pulse width can be determined with a resolution of 20ns. Other modes allow the period and interval between signals to be easily determined.

4.2.3 Timed Pulse Output Functions

For general timed pulse functions, a counter can be configured to count down with either a square wave or pulse output. With the counter in a free run mode, the CNTOUTx signal will pulse at the input CLOCK frequency divided by the Preset Value. With the counter in once-through mode, a single delayed pulse can be created by enabling a reset after latching.

4.3 ID PROM

Refer to 3.3.2 for a description of the ID PROM's function and contents. The ID PROM is a serial device and accessing it involves writing and reading a register in a sequential manner to acquire data. Figure 5 provides a general description of the code sequence necessary to read the information from the PROM. The PROM is a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet.

```
/*-------------------------------------------------------------------------*/
int read_idword (unsigned short id_addr, unsigned short *value){
  addr = 0xFE;                          /* M/MA address for IDPROM */
  id_addr = 0x80 | id_addr;             /* 80 is the read opcode for the PROM */
  write_eebyte (addr, id_addr);
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = rdval << 8;                  /* upper byte of sync code word */
  read_eebyte (addr,&rdval);            /* returns first byte of IDPROM */
  tmpval = tmpval | rdval;              /* combine bytes of sync code   */
  *value = tmpval;
  write_word(addr, 0x0000);             /* lower cs */
  return;
}
/*-------------------------------------------------------------------------*/
int write_eebyte (unsigned long addr, unsigned short value){
  write_word(addr, 0x0000);             /* insure cs is initially low */
  write_word(addr, 0x0004);             /* initialize */
  write_eebit(addr, 0x0001);            /* start bit */
  temp = value;
  for (i=0;i<=7;i++){
    write_eebit(addr, ((temp & 0x80)>>7));
    temp = (temp << 1);
  }
return;
}
/*-------------------------------------------------------------------------*/
int write_eebit (unsigned long addr, unsigned short value){
  temp = (0x0004 | (value & 0x0001));   /*  set data bit before clock */
  write_word(addr, temp);
  Delay(.000005);
  temp = (0x0006 | (value & 0x0001));   /*  set data bit & clock */
  write_word(addr, temp);
  Delay(.000005);
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebyte (unsigned short addr, unsigned short *value){
  for (i=7;i>=0;i=i-1){
    read_eebit (addr, &rdval);
    temp = temp | ((rdval&0x01) << i);
  }
  *value = temp;
  return;
}
/*-------------------------------------------------------------------------*/
int read_eebit (unsigned short addr, unsigned short *value){
  write_word(addr, 0x4);                /* lower clock bit */
  Delay(.000005);
  write_word(addr, 0x6);                /* raise clock bit */
  Delay(.000005);
  read_word (addr, value);
  return;
}
/*-------------------------------------------------------------------------*/
```

NOTE: 1. write_word and read_word are low level memory access routines.
*2. **NOT** actual code and should be treated as a modeling tool only.*

Figure 5. ID PROM Access Routine

APPENDIX A: CONNECTORS

Pin	Row A	Row B	Row C
1	/CS	GND	(/AS)
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	(/DREQ)	D20
7	A06	(/DACK)	D21
8	A07	GND	D22
9	D08	D00/(A08)	TRIGA
10	D09	D01/(A09)	TRIGB
11	D10	D02/(A10)	D23
12	D11	D03/(A11)	D24
13	D12	D04/(A12)	D25
14	D13	D05/(A13)	D26
15	D14	D06/(A14)	D27
16	D15	D07/(A15)	D28
17	/DS1	/DS0	D29
18	DTACK	/WRITE	D30
19	/IACK	/IRQ	D31
20	/RESET	SYSCLK	/DS2

Note: Signals in parentheses ( ) are not used on this module.

Figure A-1. M/MA Interface Connector Configuration

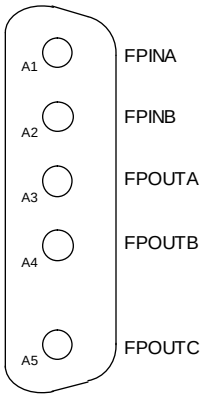

Figure A-2. Front Panel Coax D-SUB Connector Configuration

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