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i4000

Quad M-module carrier for VMEbus

User Manual

Version 1.2

CONTENTS

1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This is edition 1.2 of the i4000 user manual and applies to the following boards:
- The i4000 VME M-module carrier board without P2 of revision R4 (i4000 Rev 4)
- The i4000 VME M-module carrier board with P2 of revision R2 (i4000/R2)

The revision can be found on the printed circuit board.

1.2. PURPOSE

This manual serves as an instruction for the operation of the i4000 M-module carrier board with VMEbus interface. Some examples for using the i4000 within an APIS software environment can be found in the APIS programmers manual.

1.3. SCOPE

The scope of this manual is the usage of the i4000 M-module Carrier for VMEbus.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQuisition Platform Interface Software
ESD	Electronic Static Discharge
i4000	M-module carrier board for VMEbus
M-module	Mezzanine I/O concept according to the M-module specification
VMEbus	Versa Modular Eurocard bus

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter 2 a description of the i4000 hardware can be found. Chapter 3 covers the installation and setup of the card as well as mounting M-modules. The VMEbus interface can be found in chapter 4. In chapter 5 the operation and the usage of the i4000 is described. Finally this document contains an annex containing a bibliography, component image, technical data and the document history.

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2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The i4000 provides a compact high-performance VMEbus gateway to the M-module interface. The i4000 has a 6U form factor. Four M-modules can be mounted on the i4000.

The M-module interface of the i4000 complies with the M-module Specification. The M-module specification is ANSI approved. The M-module interface features A8, A24, D16 and D32 access types.

2.2. TECHNICAL OVERVIEW

Below an overview of the i4000 is listed.

VME interface
- A24/A16, D16/D08(EO)
- D08(O) (DYN) interrupt vector (vector unique per module)
- I(x) interrupt level (on the i4000/NP2 this is programmable per module)

M-module interface
- 4 M-module Interfaces (A08/A24, D16/D32)
- INTA software-end-of interrupt
- INTB hardware-end-of-interrupt
- INTC interrupt-vector-transfer

Connections
- Via 25 pole sub-D connector on the front of the M-module
- Via 24 pole I/O connector on the i4000 for rear I/O (only on the i4000/P2 version)
- Via P1 to VMEbus
- Via VME-P2 connector (only on the i4000/P2 version)

Note: The P2 on an i4000/P2 can be used to create an alternative I/O-path for M-modules placed on the carrier board. The M-modules must support an alternative I/O-path (usually recognizable by a 24-pole female header near the DSUB-25).

IMPORTANT: The i4000/P2 cannot be used in a VMEbus rack with monolithic backplane or a P2/J2 backplane. For these cases use an i4000/NP2 instead.

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3. Installation and Setup

3.1. Unpacking the Hardware

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. CONNECTORS

3.2.1. MOUNTING AN M-MODULE

Four M-modules can be fitted on the i4000 carrier board. To plug in a module, position the 2-row 40 pole or 3-row 60-pole M-module interface connector of the module above the 2-row header P1 of the i4000. Then push the module until the header connector is positioned and press the module with care in its place.

Note: With 3-row M-modules row C of the M-module interface connector is left unoccupied.

The module should be secured in its position using four screws (M3 * 5mm), refer to figure 1 for the positions of the mounting screws.

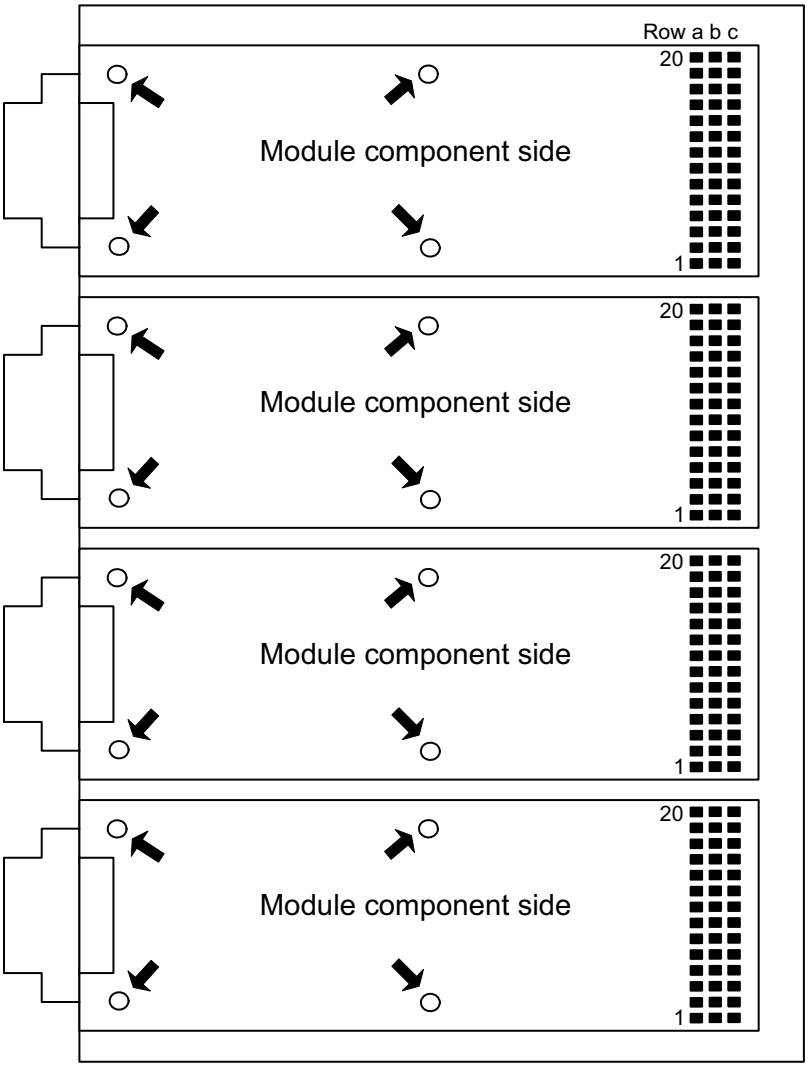

Figure 1 M-module mounting screws

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3.2.2. P2 CONNECTOR ASSIGNMENTS (I4000/P2 ONLY)

Peripherals can be connected to M-modules in two ways. On the front of the M-module a 25-pole sub-D connector (or mechanically equivalent) can be used to connect cables on the front panel of the VMEbus base board. Alternatively a 24-pole header connector interfaces the I/O signals to the base board where they are connected to the VMEbus P2 connector.

In 32-bit VMEbus systems the backplane for the P2 connector must either be removed for the i4000 slot or an i4000 without the P2 connector must be ordered. In that case the peripherals only can be connected to the M-module up front.

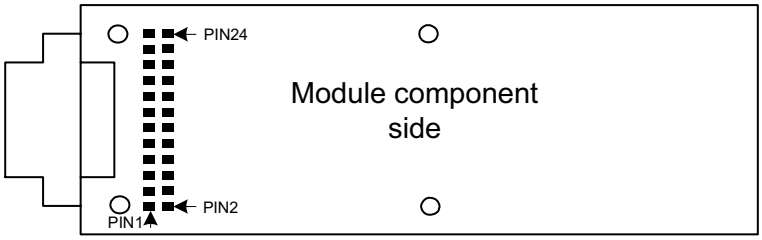

Figure 2

Every M-module has 24 pins of the P2 connector assigned. This way four modules on a base board can use this I/O path.

This division into four pads of the P2 connector enables the so called “module connector” to be plugged into the back of a 96-way shroud, mounted on the “P2-backplane”. On the 96-way connector 3 pins are not used for every module. Several manufacturers produce these “module connectors”, which can be coded and sometimes have latches.

Corresponding pins on the 96-way P2 to 24-way header connector on the module

pin	Row c	Row b	Row a
01	3	2	1
02	6	5	4
03	9	8	7
04	12	11	10
05	15	14	13
06	18	17	16
07	21	20	19
08	(24)	(23)	(22)
09	3	2	1
10	6	5	4
11	9	8	7
12	12	11	10
13	15	14	13
14	18	17	16
15	21	20	19
16	(24)	(23)	(22)
17	3	2	1
18	6	5	4
19	9	8	7
20	12	11	10
21	15	14	13
22	18	17	16
23	21	20	19
24	(24)	(23)	(22)
25	3	2	1
26	6	5	4
27	9	8	7
28	12	11	10
29	15	14	13
30	18	17	16
31	21	20	19
32	(24)	(23)	(22)

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3.2.3. M-MODULE INTERFACE CONNECTOR

The following table provides signal names for the M-module male connector that is used by the i4000. The connector consists of two rows of pins labelled rows A and B. The M-module specification also defines a third row (C). This row is rarely used and not available on the i4000. When an M-module with row A, B and C is used, row C is left unoccupied.

Pin Number	Row A	Row B
01	CS*	GND
02	A01	+5V
03	A02	+12V
04	A03	-12V
05	A04	GND
06	A05	DREQ*
07	A06	DACK*
08	A07	GND
09	D08	D00
10	D09	D01
11	D10	D02
12	D11	D03
13	D12	D04
14	D13	D05
15	D14	D06
16	D15	D07
17	DS1*	DS0*
18	DTACK*	WRITE*
19	IACK*	IRQ*
20	RESET*	SYSCLK

Location of the 40 or 60 pole female header connector on the M-module: (60 pole shown)

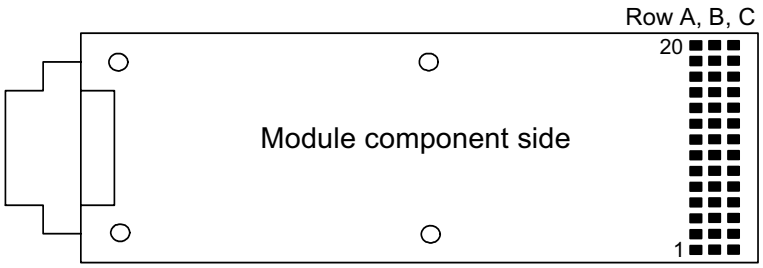

Figure 3 M-module Interface Connector

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4. VMEBUS INTERFACE

4.1. ADDRESS INTERFACE

The i4000 can be selected to accept either short addressing, using 16-bit addresses (A16) or standard addressing, using 24-bit addresses (A24).

When using short addressing up to 32 i4000 boards can be put in a single VMEbus system since the lower 11 address lines (A0-A10) are used internally on the i4000. If standard addressing is used, a larger address space is available to select the board.

The memory space occupied by the i4000 is 0x800 bytes long. This memory space is equally spread across the four modules. So each module occupies 0x200 bytes. From these 0x200 bytes address space half is used by the interrupt controller. The address space for each module is therefore 0x100 bytes long (8 bit addressing).

The address space of the i4000 is selectable using dip switches (SW1 and SW2) which are accessible even when the four module slots are occupied. When a switch is “on” the corresponding address line is a logical “zero” and when a switch is “off” the corresponding address line is “one”.

Address modifier AM4 can be used to select either standard or short memory addressing. If AM4 is “one” (the switch is in the off position) standard addressing is selected. If AM4 is “zero” (switch on) short addressing is selected. When using short addressing the address lines A16-A23 are don’t cares.

Figure 4 Address Selection

4.2. THE INTERRUPTER

The i4000 has a interrupter which is largely compatible with the MC68C153. The interrupter is a so called D08(O) type interrupter which means that the interrupter during an interrupt acknowledge cycle will put a status byte on the data lines D0-D7.

The interrupter uses a fixed interrupt level (IRQ1-IRQ7 set by SW1) for all M-modules. The i4000/NP2 also can be set to “software programmable level”, the interrupt level for an M-module has to be programmed using the control registers. Each M-module can generate its own vector.

L2	L1	L0	Interrupt level
on	on	on	software programmable level (only i4000/NP2)
on	on	off	level 1
on	off	on	level 2
on	off	off	level 3
off	on	on	level 4
off	on	off	level 5
off	on	off	level 6
off	off	off	level 7

There are two classes of interrupters which are both supported by the i4000: release on acknowledge (ROAK) or release on register access (RORA). The ROAK interrupter negates its interrupt request line in response to an interrupt acknowledge cycle. This mechanism will work with all handlers. The RORA interrupter releases its request when the handler accesses an on-board register during the interrupt service routine. The handler performs the acknowledge cycle but the interrupter does not immediately negate its request. Sometime during the service routine the handler will have to write to a register on the interrupter which causes it to negate the request.

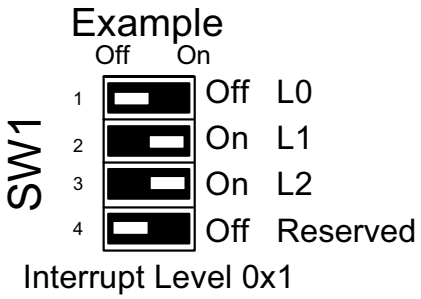

Figure 5 Interrupt request level

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4.3. DIPSWITCH LOCATIONS

The location of the dip switches to select the base address (SW2 and SW3) and the dip switch to select the interrupt request level (SW1) can be found at the following locations:

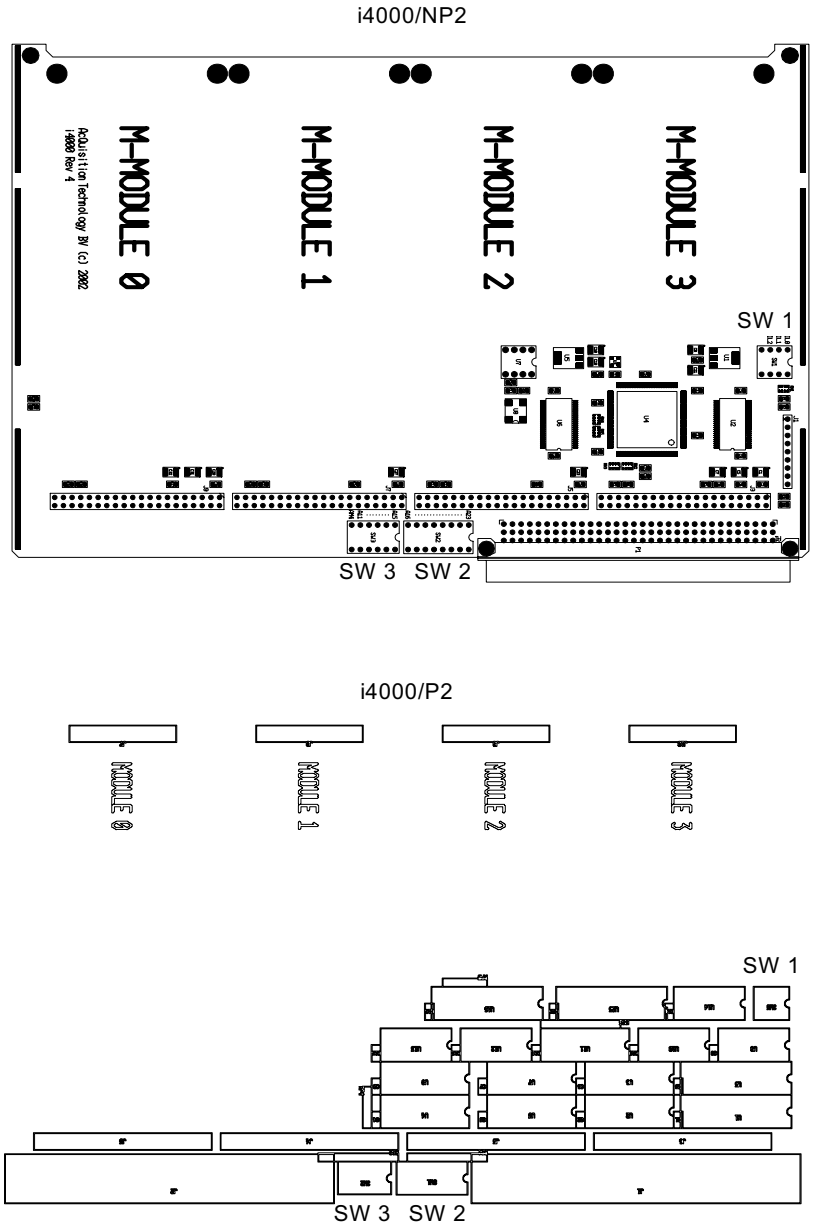

Figure 6

4.4. VMEbus P1 Connector Assignments

The following table provides signal names for the VMEbus P1 connector as used by the i4000. The connector consists of three rows of pins labelled rows A, B and C.

Pin	Row A	Row B	Row C
01	D00		D08
02	D01		D09
03	D02		D10
04	D03	BG0IN*	D11
05	D04	BG0OUT*	D12
06	D05	BG1IN*	D13
07	D06	BG1OUT*	D14
08	D07	BG2IN*	D15
09	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	
11	GND	BG3OUT*	
12	DS1*		RESET*
13	DS0*		LWORD*
14	WRITE*		AM5
15	GND		A23
16	DTACK*		A22
17	GND		A21
18	AS*		A20
19	GND		A19
20	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V		+12V
32	+5V	+5V	+5V

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5. FUNCTIONAL DESCRIPTION

5.1. BLOCK DIAGRAM

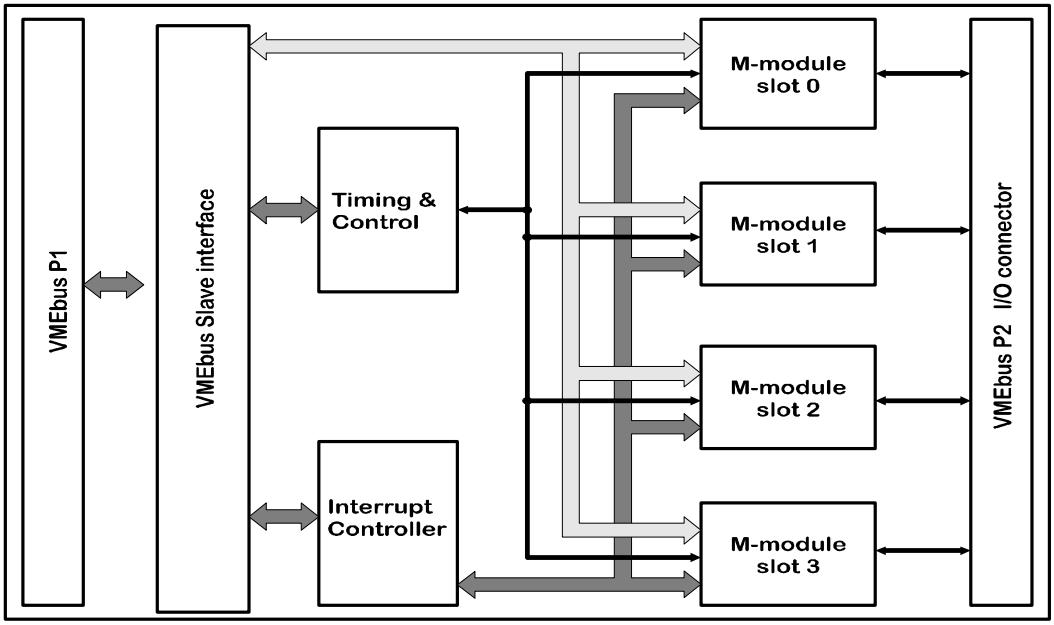

Figure 7 i4000 block diagram

The interrupt controller used on the i4000 is largely compatible with the MC68153 interrupt controller from Motorola.

The interrupt controller provides means for the modules to ask for an interrupt of the processor activity and receive service from the processor. The interrupt controller on the i4000 acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent modules.

5.1.1. REGISTER DESCRIPTION

The interrupt controller of the i4000 contains 8 programmable registers. There are four control registers (CR0-CR3) that control the operation of the interrupt controller and four vector registers (VR0-VR3) that contain the vector data used during an interrupt acknowledge cycle. Every module is assigned one register pair.

5.1.2. ADDRESS MAPPING

As mentioned before the address space occupied by the i4000 board is 0x800 bytes (A0-A10). These 0x800 bytes are divided into 4 identical spaces. Every 0x200 bytes block is assigned to a module slot. The first 0x100 bytes address space are assigned to the module itself and the second 0x100 bytes are used for the access part of the interrupt controller.

Using this method of address decoding provides an identical address map of each module on the i4000 board. This makes writing the software easier since just the base address of the module, not the base address of the i4000 has to be known. Every module has its own Interrupt-Vector and Interrupt-Control register. The 0x100 bytes from each module used to access the interrupt controller are not completely decoded. Both registers of the interrupt controller are mirrored several times within the 0x100 bytes address space. Decoding of the M-module's 0x100 bytes of address space is done on the used M-module.

Address map of the i4000

0x000..0x0ff 0x101 0x103	Module Control register (CR0) Vector register (VR0	Module 0
0x200..0x2ff 0x301 0x303	Module Control register (CR1) Vector register (VR1)	Module 1
0x400..0x4ff 0x501 0x503	Module Control register (CR2) Vector register (VR2)	Module 2
0x600..0x6ff 0x701 0x703	Module Control register (CR3) Vector register (VR3)	Module 3

The base address of a module can be calculated using the following formula:

ModuleBaseAddress = i4000BaseAddress + ModuleNumber * 0x200

EXAMPLE:

The installed base address of the i4000 is 0x800000. A module is fitted into slot 2. The module base address is then 0x800000 + 2 * 0x200 = 0x800400. When using a 32 bit master, which accesses the standard address space at address 0xff??????, the module will be accessed at address 0xff800400. The corresponding interrupt control register address is then 0xff800501.

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5.1.3. CONTROL REGISTER

Control Register

7	6	5	4	3	2	1	0
RES	RES	X/IN	IRE	IRAC	L2	L1	L0
Reset:							
u	u	u	u	u	u	u	u

Write only

L2-L0 (Interrupt level)
The least significant 3-bit field of the register determines the level at which an interrupt will be generated. These three bits are only used in the i4000/NP2 interrupt controller, if the interrupt level dipswitches are set to software irq level (all “on”). The level can be programmed from “1 to 7”.

Note: The i4000/P2 only supports interrupt levels set by dipswitches, it is advisable to program the level, set by dipswitches, also in the register. This to maintain software compatibility with other similar boards.

IRAC (Interrupt Auto-Clear)
If the IRAC is set (bit 3), IRE (bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the module interrupt request. To re-enable the module interrupt request associated with this register, IRE must be set again by writing to the control register.

IRE (Interrupt enable)
This field (bit 4) must be set (high level) to enable the module interrupt request associated with the control register. If the module asserts IRQ, but IRE is cleared, no interrupt request to the VMEbus will be generated.

X/IN* (External/Internal)
Bit 5 of the control register determines the response of the i4000 interrupt controller during an interrupt acknowledge cycle. If the X/IN* bit is cleared (low level) the interrupt controller will respond with vector data and a DTACK* signal, i.e., an internal response. If X/IN* is set, the vector is not supplied and no DTACK* is given by the interrupt controller, i.e., an external module should respond.

RESERVED
These two bits are not used in the current implementation of the interrupt controller and are reserved for future use.

5.1.4. VECTOR REGISTERS

Each module interrupt has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle, if the associated External/Internal (X/IN*) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

5.1.5. INTERRUPT CONTROLLER RESET

When a VMEbus reset is applied, the control registers of the i4000 interrupt controller are set to all zeros (low). The vector registers however are uninitialized and should be programmed before use.

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6. ANNEX

6.1. COMPONENT IMAGE

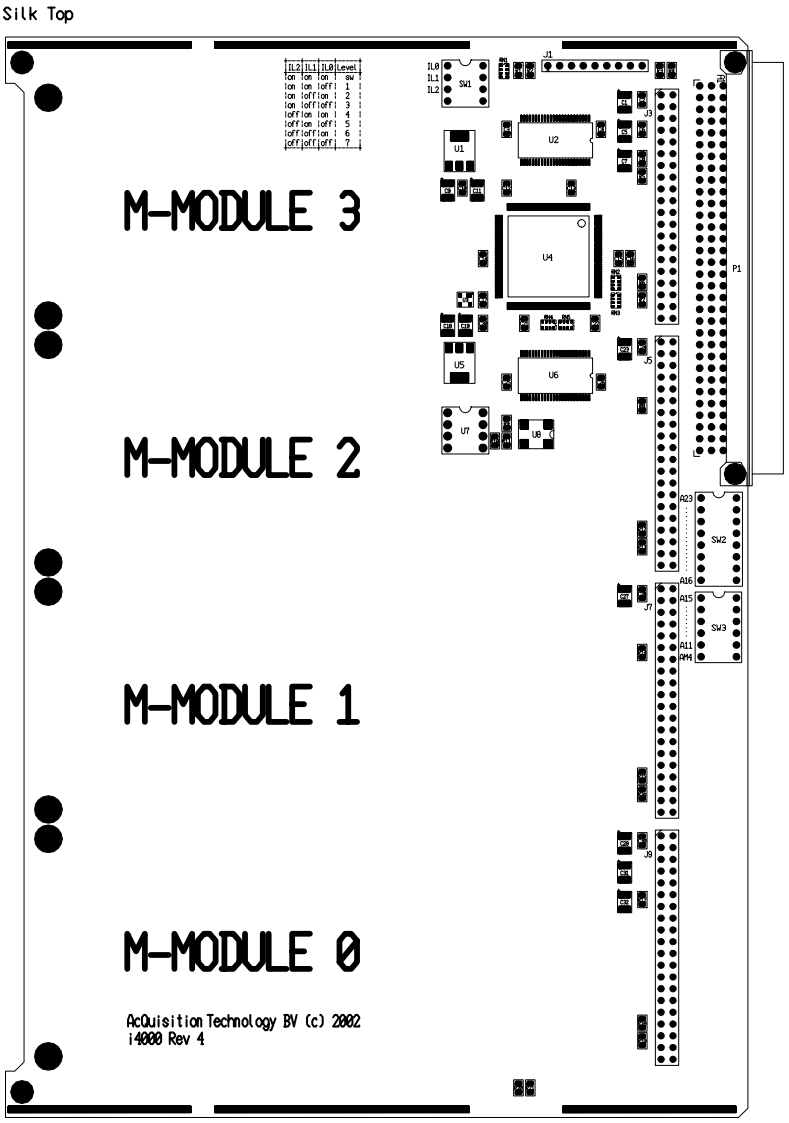

Figure 8 i4000/NP2 component view

6.2. BIBLIOGRAPHY

M-Module Standard: ANSI/VITA 12-1996, M-Module Specification;
VITA, PO Box 19658, Fountain Hills, AZ 85269, USA
Phone (1)(480)8377486
http://www.vita.com

APIS Programmer's Manual
AcQuisition Technology
P.O. Box 627, 5340 AP Oss, The Netherlands.

6.3. TECHNICAL DATA

Slots on the base-board:

Up to four modules can be plugged onto the baseboard. A huge number of baseboards in one VME system is supported.

Connection:

To base-board via VME connector.
4 x M-module interface.
M-module I/O-connector accessible through VME bracket.

Power supply:

+5VDC (+-5%), typical 300mA (without modules).
+12VDC, 0mA (without modules)
-12VDC, 0mA (without modules)

Temperature range:

Operating: 0..+60^{o}C.

Storage: -20..+70^{o}C.

Humidity:

Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release
- Version 1.1
  New layout
- Version 1.2
  General update

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