AcQuisition Technology bv

Headquarters:
Raadhuislaan 27a
5341 GL Oss

Postal address:
P.O Box 627
5340 AP Oss
The Netherlands

Phone: +31-412-651055
Fax: +31-412-651050
E-mail: info@acq.nl
Web: http://www.acq.nl

i2001

M-module Carrier for PCI Bus

User Manual

Version 1.0

Disclaimer:

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. AcQuisition Technology does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. AcQuisition Technology products are not designed, intended, or authorized for use as components in systems intended to support or sustain life, or for any other application in which the failure of an AcQuisition Technology product could create a situation where personal injury or death may occur, including, but not limited to AcQuisition Technology products used in defence, transportation, medical or nuclear applications. Should the buyer purchase or use AcQuisition Technology products for any such unintended or unauthorized application, the buyer shall indemnify and hold AcQuisition Technology and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that AcQuisition Technology was negligent regarding the design or manufacture of the part.

Printed in The Netherlands.

CONTENTS

1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This is edition 1.0 of the i2001 user manual and applies to the i2001 PCI M-module carrier board of revision R1.X, where 1 is the version of the PCB and X is the version of the PLD firmware.

1.2. PURPOSE

This manual serves as an instruction for the operation of the i2001 M-module carrier board with PCI interface. The i2001 comes with APIS based software examples, these examples are also discussed in this manual.

The i2001 is based on the PCI9030 PCI bus target interface chip of PLX Technology. For optimal performance the PCI9030 interface chip offers a wide variety of functions, a detailed description of these functions is not part of this manual.

1.3. SCOPE

The scope of this manual is the usage of the i2001 M-module Carrier for PCI Bus.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQuisition Platform Interface Software
CompactPCI	PCI with a different physical form factor
DSP	Digital Signal Processor
ESD	Electronic Static Discharge
M-module	Mezzanine I/O concept according to the M-module specification
PCI	Peripheral Component Interconnect
PLD	Programmable Logic Device

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

The jumpers are designated by a ‘J’, and a serial number. When specifying wether a jumper should be connected or removed it is referred to solely by this designation if it has only one position (e.g., ‘J5 connected’). However, if the jumper has more than one position, it is also indicated which pins are connected to each other (e.g. ‘J8, 1-2’). Pin 1 of a jumper is always marked in the configuration diagram.

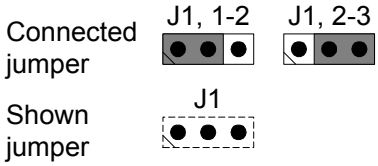

Figure 1 Example jumper nomenclature

In some illustrations jumpers are shown merely for purposes of orientation. In this case they are indicated with a dotted line. Their correct setting is described in another chapter.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter 2 a description of the i2001 hardware can be found. Chapter 3 covers the installation and setup of the card as well as mounting M-modules. In chapter 4 The operation and the usage of the i2001 is described. The i2001 is distributed with an APIS based demo application which is described in chapter 5. Finally this document contains an annex containing a bibliography, component image, technical data and the document history.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The i2001 provides a compact high-performance PCI bus gateway to the M-module interface. On the i2001, one M-module can be mounted. The M-module I/O connector is accessible through the PCI card bracket

The M-module interface of the i2001 complies with the M-module Specification. The M-module specification is ANSI approved. The M-module interface features A8, A24, D16 and D32 access types.

The PCI interface is PCI Specification 2.2 Compliant (3,3V or 5V signaling), slave only. The PCI to M-module bridge is implemented using the PCI9030 PCI Bus Target Interface Chip of PLX Technology Inc.

2.2. TECHNICAL OVERVIEW

Below an overview of the i2001 is listed.

PCI interface
- PCI Specification 2.2 Compliant Target Interface (3,3V or 5V signaling)
- Bi-directional FIFO for zero wait-state burst operation
- M-module interface runs asynchronously to the PCI clock
- Supports Big/Little Endian Byte Conversion

M-module interface
- 1 M-module Interface (A08/A24, D16/D32)
- INTA software-end-of interrupt supported

Connections
- Via Card Edge Connector to PCI bus
- Access to M-module I/O via:
  - 24 pole I/O connector on the i2001
  - M-module I/O-connector accessible through PCI bracket

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

3. INSTALLATION AND SETUP

3.1. UNPACKING THE HARDWARE

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. CONNECTORS

3.2.1. M-MODULE INTERFACE CONNECTOR

The interface between the i2001 carrier board and an M-module is realized with a 60 pole male header connector (rows A, B and C), the table below contains the pin assignment of the 60 pole connector.

Pin Number	Row A	Row B	Row C
1	CS*	GND	AS*
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	DREQ*	D20
7	A06	DACK*	D21
8	A07	GND	D22
9	D08/A16	D00/A08	TRIGA
10	D09/A17	D01/A09	TRIGB
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	DS1*	DS0*	D29
18	DTACK*	WRITE*	D30
19	IACK*	IRQ*	D31
20	RESET*	SYSCLK	DS2*

Orientation of the 60 pole male header connector on the M-module:

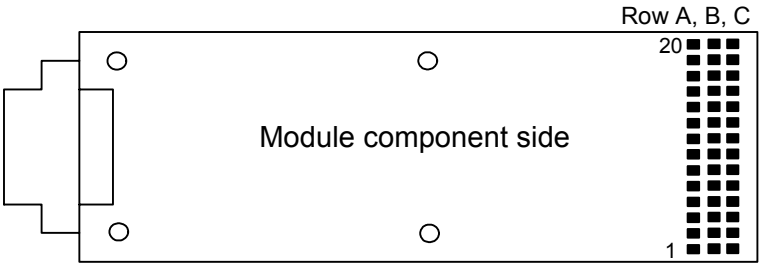

Figure 2 M-module Interface Connector

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

3.2.2. M-MODULE PERIPHERAL CONNECTOR

Some M-modules have an additional 24-pole female peripheral I/O connector. On the i2001 this peripheral connector P2 is routed to connector P2 on the M-module (one-on-one).

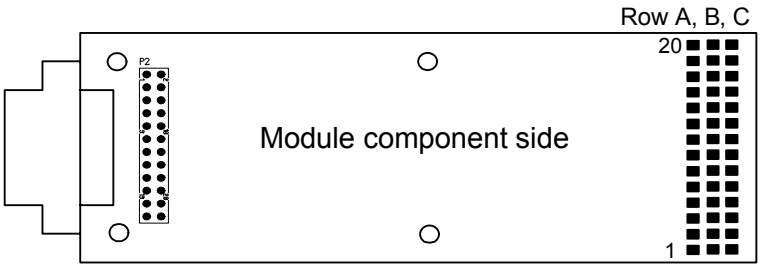

Figure 3 M-module Peripheral Connector

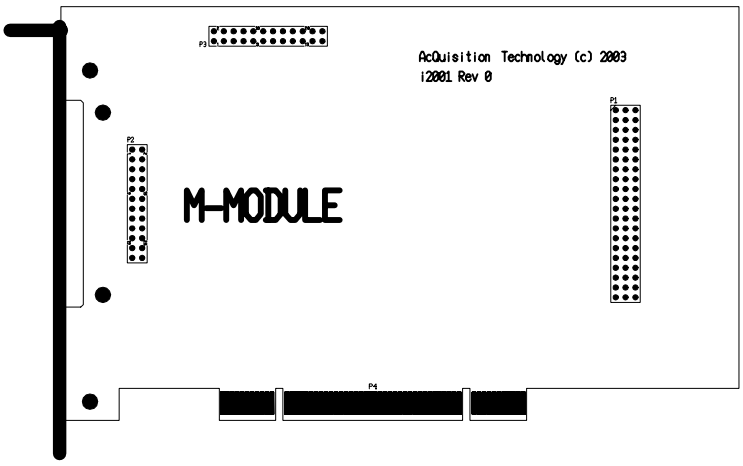

Figure 4

3.3. MOUNTING AN M-MODULE

One M-module can be fitted on the i2001 carrier board. To plug in a module position the 2-row 40 pole or 3-row 60-pole M-module interface connector of the module above the 3-row header P1 of the i2001. Then push the module until the 40 or 60-pole header connector is positioned and press the module with care in its place.

Note: With 2-row M-modules row C of the M-module interface connector is left unoccupied.

The module can be secured in its position using four screws (M3 * 5mm), refer to figure 5 for the positions of the mounting screws.

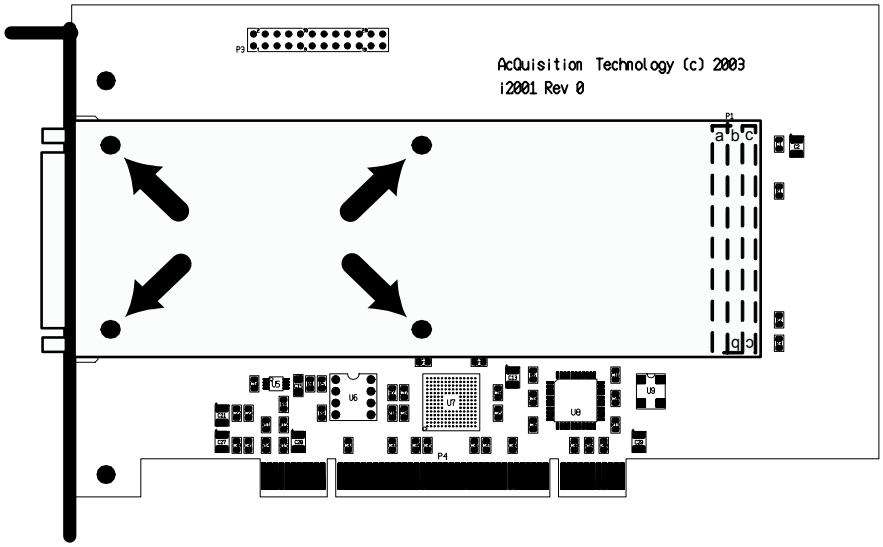

Figure 5 M-module mounting screws

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4. FUNCTIONAL DESCRIPTION

4.1. BLOCK DIAGRAM

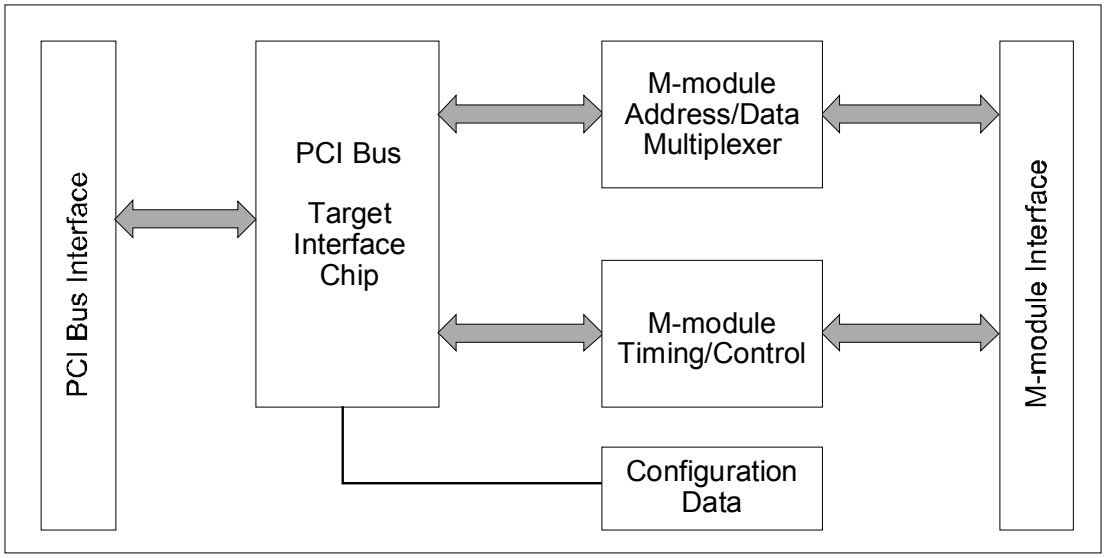

Figure 6 i2001 block diagram

4.2. PCI TO M-MODULE BRIDGE

The PCI to M-module bridge is implemented using the PCI9030 PCI Bus Target Interface Chip by PLX Technology Inc.

The PCI9030 supports both memory mapped and I/O mapped accesses from the PCI bus to the local M-module bus. Bi-directional FIFOs enable high-performance bursting on the local and PCI bus.

4.2.1. LOCAL BUS CONFIGURATION

The i2001 features programmable local bus configuration. The local busses may be either 16 or 32 bit wide and may be multiplexed or non-multiplexed. The PCI9030 also offers big/little endian byte swapping.

The PCI9030 offers four local address spaces. On the i2001 local address space 0 is standard configured for A8/D16 little endian memory mapped M-module accesses and local address space 1 for A8/D16 little endian I/O mapped M-module accesses.

The local bus data lines (LAD0-LAD31) are connected to the M-module data lines (MD0-MD31).
M-module accesses are asynchronous using the READY input of the PCI9030.

Configuration of the PCI interface and local address spaces is done through the PCI9030 configuration registers.

The table below gives an overview of the local memory map:

Local Address	Description
0x00000000	A24/D16
0x01000000	A24/D32
0x02000000	A08/D16
0x02000100	A08/D32
0x02000200	Control reg

4.2.2. INTERRUPTS

On the i2001 there are three types of interrupts, M-module interrupts, timeout interrupts and address error interrupts. M-module interrupts are connected to LINT1 of the PCI9030, timeout interrupts and address error interrupts are connected to LINT2 of the PCI9030.

The interrupt control register is used to enable and check the status of the M-module interrupt. Refer to section

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

4.2.3. CONFIGURATION EEPROM

After reset the PCI9030 reads a serial EEPROM on the card containing factory settings. Default local address space 0 of the PCI 9030 is configured for A08D16 type of M-module accesses mapped in memory space and local address space 1 is configured for A08D16 type of M-module accesses mapped in I/O space.

The table below shows the contents of the serial EEPROM on a standard i2001.

Offset	Contents	Register	Description
00	3090	Device ID	PCIIDR[31:16]
02	10B5	Vendor ID	PCIIDR[15:0]
04	0280	PCI Status	PCISR[15:0]
06	0000	PCI Command	***Reserved***
08	0801	Class Code	PCICCR[15:0]
0A	0001	Class Code / Revision	PCICCR[7:0]/PCIREV[7:0]
0C	2001	Subsystem ID	PCISID[15:0]
0E	10B5	Subsystem Vendor ID	PCISVID[15:0]
10	0000	MSB New Capability Pointer	**Reserved**
12	0040	LSB New Capability Pointer	CAP_PTR[7:0]
14	0000	(Maximum latency and Minimum Grant are not loadable)	***Reserved***
16	0100	interrupt Pin (Interrupt Line Routing is not loadable)	PCIIPR[7:0]/PCIILR[7:0]
18	4801	MSW of Power Management Capabillities	PMC[15:11,5,3:0]
1A	0001	LSW of Power Management Next Capability Pointer/Power Management Capability ID	PMNEXT[7:0] / PMCAPID[7:0]
1C	0000	MSW of Power Management Data/PMCSR Bridge Support Extension	***Reserved***
1E	0000	LSW of Power Management Control/Status	PMCSR[14:8]
20	0000	MSW of Hot Swap Control/Status	***Reserved***
22	0000	LSW of Hot Swap Next Capability Pointer/ Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]
24	0000	PCI Vital Product Data Address	***Reserved***
26	0003	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[7:0] / PVPDCNTL[7:0]
28	0FFF	MSW of Local Address Space 0 Range	LAS0RR[31:16]
2A	FC00	LSW of Local Address Space 0 Range	LAS0RR[15:0]
2C	0FFF	MSW of Local Address Space 1 Range	LAS1RR[31:16]
2E	FF01	LSW of Local Address Space 1 Range	LAS1RR[15:0]
30	0000	MSW of Local Address Space 2 Range	LAS2RR[31:16]
32	0000	LSW of Local Address Space 2 Range	LAS2RR[15:0]

Offset	Contents	Register	Description
34	0000	MSW of Local Address Space 3 Range	LAS3RR[31:16]
36	0000	LSW of Local Address Space 3 Range	LAS3RR[15:0]
38	0000	MSW of Expansion ROM Range	EROMRR[31:16]
3A	0000	LSW of Expansion ROM Range	EROMRR[15:0]
3C	0200	MSW of Address Space 0 Local Base Address (Remap)	LAS0BA[31:16]
3E	0001	LSW of Address Space 0 Local Base Address (Remap)	LAS0BA[15:0]
40	0200	MSW of Local Address Space 1 Local Base Address (Remap	LAS1BA[31:16]
42	0001	LSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[15:0]
44	0000	MSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[31:16]
46	0000	LSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[15:0]
48	0000	MSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[31:16]
4A	0000	LSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[15:0]
4C	0000	MSW of Expansion ROM Local Base Address (Remap)	EROMBA[31:16]
4E	0000	LSW of Expansion ROM Local Base Address (Remap)	EROMBA[15:0]
50	0040	MSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[31:16]
52	0002	LSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[15:0]
54	0040	MSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[31:16]
56	0002	LSW of Local Address Space 1 bus Region Descriptor	LAS1BRD[15:0]
58	0000	MSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[31:16]
5A	0000	LSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[15:0]
5C	0000	MSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[31:16]
5E	0000	LSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[15:0]
60	0000	MSW of Expansion ROM Bus Region Descriptor	EROMBRD[31:16]

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

Offset	Contents	Register	Description
62	0000	LSW of Expansion ROM Bus Region Descriptor	EROMBRD[15:0]
64	0200	MSW of Chip Select 0 Base Address	CS0BASE[31:16]
66	0281	LSW of Chip Select 0 Base Address	CS0BASE[15:0]
68	0000	MSW of Chip Select 1 Base Address	CS1BASE[31:16]
6A	0000	LSW of Chip Select 1 Base Address	CS1BASE[15:0]
6C	0000	MSW of Chip Select 2 Base Address	CS2BASE[31:16]
6E	0000	LSW of Chip Select 2 Base Address	CS2BASE[15:0]
70	0000	MSW of Chip Select 3 Base Address	CS3BASE[31:16]
72	0000	LSW of Chip Select 3 Base Address	CS3BASE[15:0]
74	0030	Serial EEPROM Write-Protected Address Boundry	PROT_AREA[7:0]
76	0000	LSW of Interrupt Control/Status	INTCSR[15:0]
78	0078	MSW of PCI Target Response, Serial EEPROM, And Initialization Control	CNTRL[31:16]
7A	4000	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[15:0]
7C	0024	MSW of General Purpose I/O Control	GPIOC[31:16]
7E	9000	LSW of General Purpose I/O Control	GPIOC[15:0]

WARNING: Reprogramming of the serial EEPROM is strongly discouraged because improper EEPROM contents may cause system boot problems which may require EEPROM replacement.

4.3. M-MODULE INTERFACE

The i2001 provides an M-module interface to a PCI based platform. The wide range of standardized M-modules includes not only process I/O modules but also field buses, DSP and motion control modules as well as special-purpose functions.

The i2001 has the following M-module features:
- 3-row M-modules supported
- 2-row M-modules supported
- A08/A24, D16/D32 address/data range
- INTA supported

4.3.1. STANDARD ACCESSES

The standard M-module interface has an 8-bit address bus. Timing during access is determined solely by the signal SELECT* and DTACK*. This substantially decreases the circuit complexity on the M-modules. On M-modules supporting extended address space, the standard M-module access can be used as an I/O cycle to distinguish between memory type access and register type access.

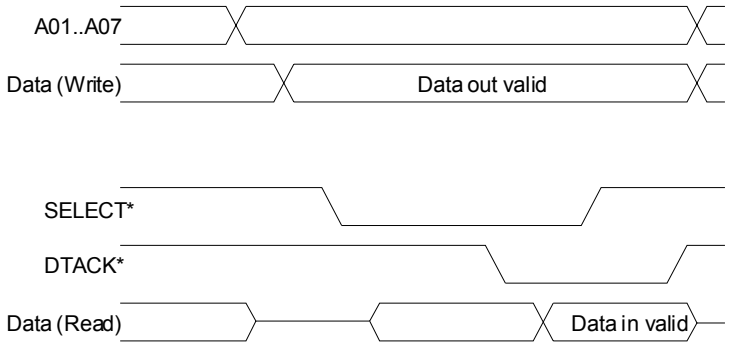

Figure 7 Standard read/write transfer

4.3.2. EXTENDED ACCESSES

The extended address space enables M-modules to be used for applications extending beyond typical I/O functions. The i2001 supports M-modules with an address bus up to 24-bit. The address information is transferred across the data bus in multiplexed mode, reducing the number of pins required. An additional line AS* indicates the current use of the bus. The standard M-module store cycle is embedded in the address transfer cycle.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

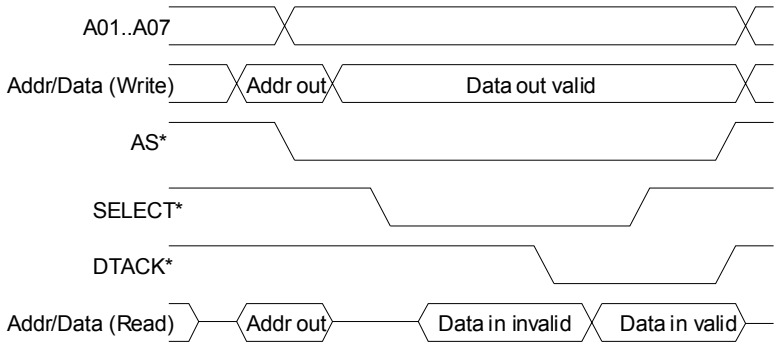

Figure 8 Extended read/write transfers

By mapping both standard and extended M-module access in a different address space as seen from the carrier board, a distinction between a standard and extended M-module access can be made. The table below gives an overview of the local address map in relation to the M-module access type.

Local Address	M-module Access Type
0x00000000	A24/D16
0x01000000	A24/D32
0x02000000	A08/D16
0x02000100	A08/D32

Note: Since the standard M-module access is embedded into the extended M-module access, it is also possible to access a standard M-module in the A24 address range.

4.3.3. THE INTERRUPT STATUS CONTROL REGISTER

With the interrupt status control register the interrupts of the i2001 can be controlled. The interrupt status control register is located at local address 0x02000200.

IC_REG Address: 0x02000200

15	1	0
not used		
reset:	AE	T0
	0	0

Read / Write

AE Address error
When asserted, the PCI bus master has requested single bytes in different words of a double word. This error only occurs in D32 mode and generates an address error interrupt which is connected to LINT2 of the PCI9030. Clear error by writing a ‘0’ to it.

TO Timeout
When asserted, a transfer timeout has occurred and a timeout interrupt has been generated. Clear pending interrupt by writing a ‘0’ to it. The timeout interrupt is connected to LINT2 of the PCI9030.

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

5. SOFTWARE SUPPORT

The i2001 comes with an APIS based application that scans the PCI bus for M-modules (modscan). This chapter gives a short description of APIS and the usage of the modscan application.

5.1. APIS

AcQ produces and markets a large number of standard M-modules varying from networking and process I/O to motion control applications. Physically, the M-modules are supported by a large number of hardware platforms: VMEbus, PCI, CompactPCI as well as a wide variety of operating systems: OS-9, Windows NT, Linux etc.

APIS (AcQ's Platform Interface Software) offers a way to program platform independent applications, example- and test software for controlling hardware. Application software written for APIS only needs re-compiling for a particular platform and must be operational with little effort (provided that the application is operating system independent). APIS support for i2001 is currently available for DOS, Windows 95/98/2000/ NT/XP, QNX, Linux and Solaris. Please check our website for up-to-date APIS support information. Refer to the APIS Programmer's Manual for more information about APIS.

5.2. MODSCAN

Modscan is an APIS based application that scans the PCI bus for M-modules. The program can be called from the command line and detects all AcQuisition Technology's PCI based M-module carrier boards (i2000, i2001, i3000, i3100, etc.). The IDs of the M-modules present on the carrier are displayed. When an M-module does not have an identification EEPROM, ‘Unknown M-module' is displayed. If a slot on a carrier is not occupied with an M-module, it is not displayed in the output.

The display output of modscan may look as follows:

```
M-module scan software by
AcQuisition Technology B.V. 2002

Slot 0: M321
Slot 1: M302
Slot 3: Unknown M-module
Slot 4: M395

Program closed
```

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands

6. ANNEX

6.1. BIBLIOGRAPHY

M-Module Standard: ANSI/VITA 12-1996, M-Module Specification;
VITA, PO Box 19658, Fountain Hills, AZ 85269, USA
Phone (1)(480)8377486
http://www.vita.com

PCI9030 PCI Bus Target Interface Chip Data sheet
PLX Technology INC, 390 Potrero Ave, Sunnyvale, CA 94086, USA.

PCI Local Bus Specification Revision 2.1.
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344

PCI BIOS Specification Revision 2.1.
PCI Special Interest Group, 2575 NE Kathryn #17 Hillsboro, OR 97124, USA
Phone (1)(503)6936232, Fax (1)(503)6938344

PCI System Architecture, Third Edition
Tom Shanley/Don Anderson
ISBN: 0-201-40993-3

6.2. COMPONENT IMAGE

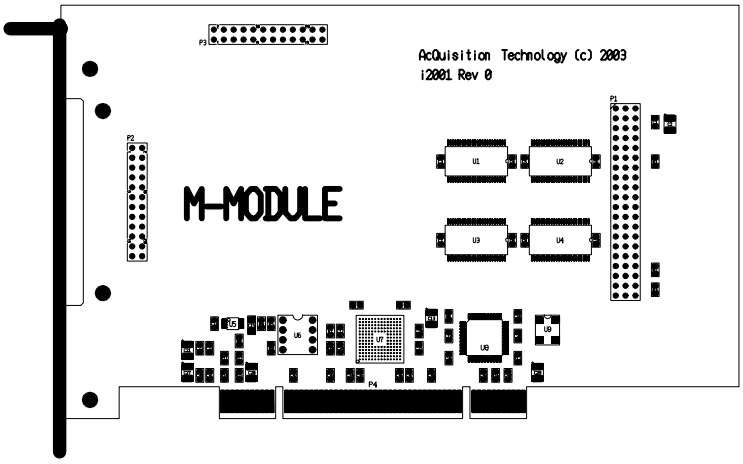

Figure 9 i2001 component view

6.3. TECHNICAL DATA

Slots on the base-board:
Requires one PCI slot.

Connection:
To base-board via PCI connector.
1 x M-module interface.
M-module I/O-connector accessible through PCI bracket.

Power supply:
+5VDC ±10%, typical 250mA (without an M-module mounted).

Temperature range:
Operating: 0..+60EC.
Storage : -20..+70EC.

Humidity:
Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release

AcQuisition Technology bv
P.O. Box 627, 5340 AP
Oss, The Netherlands